Power Contracts:Provably Complete Power Leakage Models for Processors

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ABSTRACT
The protection of cryptographic software implementations against power-analysis attacks is critical for applications in embedded systems. A commonly used algorithmic countermeasure against these attacks is masking, a secret-sharing scheme that splits a sensitive computation into computations on multiple random shares. In practice, the security of masking schemes relies on several assumptions that are often violated by microarchitectural side-effects of CPUs. Many past works address this problem by studying these leakage effects and building corresponding leakage models that can then be integrated into a software verification workflow. However, these models have only been derived empirically, putting in question the otherwise rigorous security statements made with verification.

We solve this problem in two steps. First, we introduce a contract layer between the (CPU) hardware and the software that allows the specification of microarchitectural side-effects on masked software in an intuitive language. Second, we present a method for proving the correspondence between contracts and CPU netlists to ensure the completeness of the specified leakage models. Then, any further security proofs only need to happen between software and contract, which brings benefits such as reduced verification runtime, improved user experience, and the possibility of working with vendor-supplied contracts of CPUs whose design is not available on netlist-level due to IP restrictions. We apply our approach to the popular RISC-V IBEX core, provide a corresponding formally verified contract, and describe how this contract could be used to verify masked software implementations.

KEYWORDS
Power side-channel, Leakage model, Verification, Contract, Domain-specific language, Masking, Probing security

1 INTRODUCTION
Physical side-channel attacks such as power or EM analysis allow attackers within proximity of a device to learn sensitive information like cryptographic keys [32, 47]. One of the most widely used algorithmic countermeasures for protecting a cryptographic implementation against these kinds of attacks is masking [14, 27, 31]. Masking is a secret-sharing technique that splits input and intermediate variables of cryptographic computations into \( \delta \geq t + 1 \) random shares such that the observation of up to \( t \) shares does not reveal any information about their corresponding unmasked value. Masking schemes typically rely on certain assumptions, such as independent computations producing independent side-channel leakage. However, the structure of a CPU architecture can violate these assumptions and introduce additional leakage effects [15, 18, 25, 41, 45]. Such leakage is often referred to as order-reducing leakage because it induces a security loss and thus a gap between formal security assurance and practical resilience. The physical characteristics of CMOS gates are relatively well understood and give rise to extended leakage models, which allow constructing hardware implementations that reliably mitigate order-reducing leakage [17, 20, 35, 36]. Similarly, when designing masked software implementations of cryptographic algorithms, knowing the concrete power side-effects of different instruction types is indispensable. It allows developers to optimize the performance of masked implementations by simplifying the otherwise trial-and-error hardening process [9].

State of the Art. Many works address the problem of characterizing and understanding the leakage behavior of instructions. These can be divided into two categories: works that use empirical methods to determine side-channel leakage, and works that use formal verification approaches to verify side-channel resilience.

On the empirical side, the measurement of a CPU’s power consumption combined with a subsequent analysis using statistical methods is a straightforward approach to determine whether cryptographic software is correctly masked. Any observed leakage effects can be reverse-engineered and taken into account in hardened versions of the respective masked software implementations [1, 23, 24, 38, 39, 45, 50]. The authors of ELMO [39] characterize leakage behavior by selecting “explanatory variables”, e.g., operands of assembly instructions and determining whether the variables contribute to the measured leakage using statistical tests. Variables with a correlation to measured leakage form a “leakage model”. Such a
model specifies the side-effects of a (sequence of) assembly instructions which may be exploited using for example Differential Power Analysis (DPA) [33, 40] to learn information about processed cryptographic keys. However, manual selection of variables, statistical methods and physical measurements bear potential for incomplete models which do not specify leakage of data which in practice could be exploited. Specifically, the restriction to sequences of three instructions in [39] may miss leakage effects spanning between two load instructions spaced by multiple instructions as observed in [9, 45]. Similar issues exist with other works that try to generalize power side-channel leakages that are often reported on a variety of devices in generic leakage models [9, 10, 39]. Any work building upon empirical or generalized models, e.g., ELMO [39], ROSITA [50] and TORNADO [11] only report, respectively protect against, vulnerabilities and leakages which are part of the model. Hence, all existing empirical approaches either require high practical effort or cannot guarantee completeness, thereby reducing the confidence in security assessments [5, 26, 41].

On the formal verification side, several works verify the security of masked software under specific masking-related security notions. MaskVerif performs algorithmic software masking verification using generic leakage models and supports the commonly accepted $t$-N and $t$-SNI security notions [7, 8]. scVerif improves upon this and verifies the absence of order-reducing leakage in user-provided leakage models for assembly instructions [9]. However, the security assurance still relies on the completeness of the used leakage models, as it is the case for pure empirical approaches.

Coco is a formal masking verification tool that avoids modeling the leakage by directly working with the processor netlist [25, 26, 30]. Their approach considers the leakage of every gate in an extended hardware leakage model and captures a wide range of microarchitectural side-effects. However, their method requires the processor’s netlist, which may not be available.

Hardware-software contracts have previously been used to verify speculative and timing related side-channel resilience [29]. The contracts presented in this paper are more flexible and apply to arbitrary side-channel behavior, devices and software implementations. Their close correspondence to the respective ISAs facilitates understanding by users.

**Our Contribution.** We answer to the question of leakage model completeness and establish end-to-end (E2E) security for software executing on a processor. First, we introduce a *contract* between the hardware and the software that defines precise semantics and models side-channel behavior of assembly instructions. We then establish a technique to verify *compliance* of a processor with a contract. A processor is compliant when the leakage of each of its gates and the semantic of instruction is correctly specified in the contract. Put vice-versa, we prove the contract’s model of instructions correct and its model of leakages complete. We pave the way for provable E2E security by defining software compliance for threshold probing security notions so that the approach of Barthe et al. [9] can be easily mapped to our slightly different language for contracts. We combine hardware compliance and software compliance to prove E2E security: *any* compliant software is secure w.r.t. *all* microarchitectural power side-channel leakage of *any* compliant CPU. Compared to related work, our approach comes with benefits such as more rigorous (practical) security statements, simplified software verification workflows, and the possibility of working with vendor-supplied contracts of CPUs whose design is not available on netlist-level due to IP restrictions. Our contributions also enable the construction of reliable hardened processors, as users can specify the desired leakage model in a contract and modify the CPU implementation to achieve compliance for fixed contracts. We emphasize that the intermediate contract layer enables for the first time portability of secure implementations across processors and improves the separation of secure hardware and software development in general. This separation also optionally allows the creation of vendor-supplied CPU contracts whose leakage specification is “high-level” on purpose to avoid potential IP-related issues yet modeling all real leakages in the actual hardware.

1. **Contracts.** We introduce an intuitive and industry-grade domain-specific language (DSL) called Genoa. Genoa allows specifying Instruction Set Architecture (ISA) semantics and device-specific leakages in contracts. Genoa extends the long-standing Sail language [4] to support leakage specifications. The RISC-V foundation recently picked Sail as the official tool to specify the reference RISC-V ISA and all standard extensions [42, 49]. Models for multiple architectures (e.g., ARM) exist, which can be freely adopted and compiled to software emulators [4]. We reuse existing models as the basis for contracts, augmenting them with leakage specifications and providing an interface for our verification tool. We show that whenever a program is secure with respect to a contract, its concrete execution on a compliant processor is also secure, i.e., no order-reducing leakage can occur. We emphasize that our contracts also support higher-order masking, branching, and secret-dependent memory accesses needed for masked table lookups [16].

2. **Hardware Compliance.** We present a method to automatically verify the compliance of a processor with a contract. Verification ensures that the leakage of every gate is captured by a leakage specification in the contract and that the contract specifies correct instruction semantics. Our methodology is based on the intuition that if the contract properly models the hardware, then any leakage arising in the hardware can be computed from leakage produced during an execution in the contract. It is hence up to the contract designer if they want to create exact specifications for every leakage of a CPU design, a high-level specification that does not contain any information about the CPUs microarchitecture (while still covering all real leakages), or any trade-off between the two. The verification encodes both hardware and contract execution, respectively leakage, as SMT formulas and checks for model gaps using the SMT solver Z3 [6, 19]. If the solver finds no cases where a hardware leakage is not modeled from the contract leakage, we have proven hardware compliance.

3. **Case Study.** We implement our methods in a tool and apply them to the popular RISC-V IBEX core [34], resulting in a verifiably complete contract for a wide range of instructions that are commonly used for cryptographic implementations. IBEX is a low-end processor, suitable for embedded or IoT applications that require cryptographic computations. Our analysis is focused on gate-level power leakage and we consider features such as speculative execution or data caches as out of scope since they are mostly deactivated while executing masked programs.
We introduce preliminaries for side-channel security. Hardware wires without any loss due to measurement noise [5, 20, 31]. The power consumption of CMOS gates depends on the charges effects are also observable in hardware. We define our extended \( \lambda \) allows an idealized adversary to observe the value of any wire \( \lambda_g(a_{j+1}, a_j) = g(\sigma_{j+1}^h) \). This sufficiently captures any real-world transition leakage function computable from the old and new gate values. In addition to these main phenomena, there are glitches caused by propagation delay in the temporary logic states of combinatorial circuits within one clock cycle (and thus rather ephemeral) [37] and couplings caused by inductive coupling of adjacent wires [17]. These can be modeled by defining \( \lambda_g(a_{j+1}, a_j^h) \) for non-register gates as the concatenation of all possible values the gate \( g \) could take on due to these effects. We use \( L^h_{0:m} \) to denote the observable gate-level leakage throughout the execution starting in state \( \sigma_n^h \) and ending in state \( \sigma_m^h \). While the techniques described in the following apply to all effects, for the purpose of this paper, we focus on value leakage and transition leakage. Hence, we define \( L^h_{0:m} = \{\lambda_g(a_{j+1}, a_j^h) \mid g \in G, 1 \leq j < m\} \).

## 2 SIDE-CHANNEL RESILIENCE

We introduce preliminaries for side-channel security. Hardware circuits and their power side-channel leakage are modeled in Section 2.1. In Section 2.2, we recall the masking countermeasure and the formal notions of provable side-channel resilience.

### 2.1 Hardware Model and Gate-level Leakage

Processors are digital hardware circuits which can be modeled using labeled directed graphs. For any given circuit \((G, W, L)\), we say that \( G \) is the set of gates, \( W \subseteq G \times G \) is the set of wires connecting the gates, and \( L : G \rightarrow \{0, 1\} \) is a labeling defining the type \( \tau \in T \) of each gate \( g \in G \). The types \( T \) depend on the technology that realizes the circuit. In addition to combinational gates we only require that the technology contains an input type \( \tau_{in} \) and a register type \( \tau_{reg} \). Input gates only have outgoing wires, and register gates only have one incoming wire. Additionally, every cyclic path in the circuit contains at least one register gate. The state of a circuit is completely defined by the values of its inputs and registers, referred to as locations, denoted with \( V^h = \{ g \in G \mid L(g) \in \{\tau_{in}, \tau_{reg}\} \} \). Superscript \( h \) is for hardware, later we use \( c \) for contract. Hardware states are denoted with \( \sigma^h \in \mathbb{B}[V^h], \) with optional subscripts. Any location \( \sigma^h \in V^h \) just returns the appropriate bit of the state. Any gate \( g \) is a function of a state, \( i.e., g : \mathbb{B}[V^h] \rightarrow \mathbb{B} \) where gate \( g \in G \setminus V \) combines state bits according to its type \( \tau \).

The execution of a circuit happens in clock cycles. For a state \( a_j \), we denote the next state as \( a_{j+1}^h \). The registers of the next state have values reflecting the values of their inputs in the previous cycle, \( i.e., g(\sigma_{j+1}^h) = g'(a_j^h) \) with \( g'(a_j) \in W \), whereas the next state of circuit inputs is determined by the environment.

We now proceed to define the power side-channel leakage that is exposed to an adversary. The root cause of power side-channels is that CMOS logic draws power, or emits electromagnetic radiation, mainly if a transistor switches its state. Thus, CMOS gates have a data-dependent power consumption. The leakage behavior of CMOS gates themselves is relatively well understood and can be modeled by a few simple leakage effects which allow an (idealized) probing adversary to observe the (intermediate) values of gates and wires without any loss due to measurement noise [5, 20, 31]. The seminal work of Ishai et al. [31] introduced value leakage which allows an idealized adversary to observe the value of any wire connected to a gate at the beginning or end of a cycle, \( i.e., \) its stable signal. The value leakage \( \lambda_g \) exposed by gate \( g \) is its value \( \lambda_g(a_j) = g(\sigma_j^h) \) in the state \( \sigma_j^h \). Besides value leakage, additional leakage effects are also observable in hardware. We define our extended probing model in close relation to the robust probing model of Faust et al. [20]. Transition leakage refers to the phenomenon that the power consumption of CMOS gates depends on the charges (state) of the gate before computation. As such, transition leakage allows observing whether the value of a gate changed during a clock cycle but also whether the value changed from zero to one or vice-versa. Formally, our idealized adversary is able to observe the initial value and the resulting value of each gate. The observable gate leakage is then the concatenation of the old and new gate values, \( i.e., \lambda_g(a_{j+1}, a_j) = g(\sigma_{j+1}^h) \). This sufficiently captures any real-world transition leakage function computable from the old and new gate values. In addition to these main phenomena, there are glitches caused by propagation delay in the temporary logic states of combinatorial circuits within one clock cycle (and thus rather ephemeral) [37] and couplings caused by inductive coupling of adjacent wires [17]. These can be modeled by defining \( \lambda_g(a_{j+1}, a_j^h) \) for non-register gates as the concatenation of all possible values the gate \( g \) could take on due to these effects. We use \( L^h_{0:m} \) to denote the observable gate-level leakage throughout the execution starting in state \( \sigma_n^h \) and ending in state \( \sigma_m^h \). While the techniques described in the following apply to all effects, for the purpose of this paper, we focus on value leakage and transition leakage. Hence, we define \( L^h_{0:m} = \{\lambda_g(a_{j+1}, a_j^h) \mid g \in G, 1 \leq j < m\} \).

### 2.2 Provable Security and Simulatability

Applying masking to a cryptographic algorithm requires to replace the primitive operations (e.g., logical conjunction, exclusive or, addition) by masked computations, often called gadgets, which compute the same operation securely on shares [28, 31, 43, 48]. The challenge in the design and implementation of gadgets is to maintain the security of the secret-sharing: it must remain information theoretically impossible to learn the secrets or intermediate values by observing up to \( t \) leakages caused by the gadget. In sufficiently noisy environments this leads to an exponential gain of security in the order of \( t \) [13, 46]. However, many works do not take the full gate-level leakages into account, resulting in implementations that are exploitable at a lower-than-advertised security order. Especially for masked software, the resulting gap in the security assurance allows to break the implementation by observing, e.g., transition leakage of the processor executing the program [5, 35, 44]. This work aims to reduce the gap by enabling software security assessments to include the complete set of gate-level leakages.

We give an overview of the notation associated with masking, and formalize gadgets and their security. Masking heavily relies on random variables. We write the names of random variables in lower-case, e.g., \( x_i \), and use lowercase boldface names for sets of variables, e.g., \( x = [x_0, \ldots, x_n] \). Each random variable \( x_i \) respectively set \( x \), is associated with a probability distribution \( \Pr \{ x_i \} \), respectively \( \Pr \{ x \} \). Each secret \( x_i \) is encoded (masked) using \( d > t \) shares and we write \( \tilde{x} = (x_i^0, \ldots, x_i^d) \) for the shares which encode \( x_i \), where \( x_i^j \) denotes for \( 0 \leq i < n \) and \( 0 \leq j < d \) the \( j \)th share of the \( i \)th secret. The superset of all shares is denoted by \( \tilde{x} = (\tilde{x}_0, \ldots, \tilde{x}_n) \).

A gadget operates on input tuple \((\tilde{x}, r, p)\) returning tuple \((\tilde{y}, o, L)\), each consisting of random variables. The input shares \( \tilde{x} \) are a set of \( t \)-wise independent encodings \( \tilde{x} \), each encoding a secret variable \( x_i \), \( r \) represents a set of independent and uniformly random variables, \( p \) are public inputs independent of secrets. The output of a gadget consist of output shares \( \tilde{y} \), public outputs \( o \), and observable
leakage $\mathcal{L}$. Each individual output is a random variable $y_j^t$ (respectively $o_i$) and computed as a function of the gadget’s inputs, i.e., $y_j^t = f_j^t(\mathbf{x}, r, p)$. During its execution a gadget produces observable leakage $\mathcal{L} = \{a_0(\mathbf{x}, r, p), \ldots, a_m(\mathbf{x}, r, p)\}$, which an attacker can observe, e.g., through power measurements. The attacker’s goal is to learn information about the unshared secret inputs $x$.

Threshold non-interference ($t$–NI) and strong threshold non-interference ($t$–SNI) are two prominent security notions for proving the security of gadgets against idealized adversaries [7, 8]. These have been extended in [9] into Stateful $t$–(S)NI to incorporate that physical execution involves state and public in- and outputs. Security of gadgets in these notions is shown by proving that the observations an attacker makes can be simulated without knowing the secret values, thereby proving that no information can be gained from $t$ observations. In the following, we formalize what it means to simulate random variables, and restate $t$–NI and $t$–SNI.

**Definition 1 (Simulation Procedure).** Let $c$ and $h$ be sets of possibly related random variables and $r$ be a set of independent and uniformly distributed variables. The simulation procedure $S : \text{Dom}(c \cup r) \rightarrow \text{Dom}(h)$ (simulator for short) samples the random variables $r$ to simulate the distribution of $h$ from $c$. We say that simulator $S$ simulates $h$ from $c$ and $r$ if $\Pr[S(c, r)] = \Pr[h]$.

Importantly, the variables $c$ and $h$ are not necessarily independent, meaning $\Pr[h \mid c]$ could be different from $\Pr[h]$, i.e., their distributions are somehow related. This is the central in the definitions of Stateful $t$–NI and $t$–SNI, however, we introduce a non-probabilistic way of modeling (instead of simulating) the outcome of a computation from a related but different value.

**Definition 2 (Modeling Function).** Let $f_H : H \rightarrow V$ and $f_C : C \rightarrow U$ be deterministic functions. We say that a deterministic function $f_S : U \rightarrow V$ is a modeling function which models $f_H$ from $f_C$ under deterministic relation $\Psi : H \times C \rightarrow \mathcal{B}$ whenever

$$\forall h \in H, c \in C : \Psi(h, c) \Rightarrow f_S \circ f_C(c) = f_H(h).$$

(1)

Definition 2 is strong: whenever modeling function $f_S$ models $f_H$ then it also simulates it, captured by Lemma 1.

**Lemma 1 (Modeling Functions Simulate).** Let $h$ and $c$ be sets of possibly dependent random variables with deterministic function $f_H$ computing a set of dependent random variables $v$ and function $f_C$ computing dependent random variables $u$. If function $f_S$ models $f_H$ from $f_C$ whenever $\Psi(h, c)$ then it also simulates $v$:

$$\Pr[f_S \circ f_C(c) \mid \Psi(h, c) = \top] = \Pr[h \mid \Psi(h, c) = \top].$$

(2)

Stateful $t$–(S)NI requires a probabilistic simulator to simulate observations on leakage or outputs shares independently of secrets and a function modeling output public outputs from public inputs.

**Definition 3 (Stateful $t$–(S)NI [7–9]).** Gadget $G(\mathbf{x}, r, p) = (\mathbf{y}, o, L)$ is Stateful $t$–(S)NI if for every set $s \subseteq L \cup \mathbf{y}$, with $|s| \leq t'$, there exists a subset of input shares $\subseteq \mathbf{x}$, with $|s \cap \mathbf{x}| \leq t'$ $t$, a set of uniformly random variables $r'$, a modeling function $F : \text{Dom}(p) \rightarrow \text{Dom}(o)$ modeling public outputs $o$ from public inputs $p$ and a simulator $S : \text{Dom}(s', r', p) \rightarrow \text{Dom}(o)$ simulating observations $c$ from a subset of shares $s$, random $r'$ and public inputs $p$ such that $\Pr[S(s', r', p), F(p)] = \Pr[c, o]$ and $o = F(p)$. For $t$–NI $t' = |s|$ while the stricter $t$–SNI notion requires $t' = |c|$.}

The tool scVerif allows proving software gadgets secure under these notions for custom definitions of the observable leakage behavior $\mathcal{L}$ [9]. However, to prove security with respect to gate-level leakage, the provided model of $\mathcal{L}$ must capture absolutely all gate-level leakages of the CPU executing a gadget. In case a gate-level leakage is modeled incorrectly, the tool could assert security although the gadget can be broken with less than $t$ observations at the gate-level. As analyzed by Balasch et al. [5], such leakage may halve the security order, i.e., $t' = \frac{t}{2}$. Even worse, Gigerl et al. report protection losses that scale with the number of processor pipeline stages [26]. Our work mitigates such losses by verifying that all gate-level leakages are modeled.

## 3 HARDWARE-SOFTWARE CONTRACTS

A contract defines the instruction semantics and exposed side-channel information of a processor from the perspective of a software developer, i.e., which data is leaked via power side-channels when an instruction is executed in conjunction with the semantic of the instruction. Contracts must specify correct instruction semantics to be able to express accurate data leakage. Besides the instruction perspective contracts allow to execute and thereby model entire programs. In practice, a contract is a user-supplied text file containing specifications of instructions written in GENOA.

In Sections 3.1 and 3.2, we describe how to build a contract which completely captures the leakage exposed by every single gate of a processor. In Section 3.3 we define how to verify the security of masked software against the model specified in a contract. We then turn towards the question of model completeness: In Section 3.4 we define compliance, a property which connects gate-level leakage of a processor to the leakage model specified in a contract. Finally, we prove E2E security by showing that if a processor’s hardware complies with a contract, the contract models all gate-level leakages. Proving the security of a program against the leakage model specified in the contract implies that the same order of security is achieved when executed on real, compliant hardware. Section 4 introduces a way to check compliance of processors and contracts.

### 3.1 Expressing Contracts in GENOA

GENOA extends SAIL by a dedicated `leak` statement to express that specific values are observable through a side-channel. For example, a statement of the form `leak(val1, val2)` indicates that the processor may leak any combination of the source operands, i.e., any value that can be computed using these operands. Users are free to specify more fine-grained leakage using concrete functions, e.g., the Hamming-Distance.

Barthe et al. applied this concept in [9] to a custom DSL but leave the error-prone and time-consuming task of modeling semantic and leakage to the user. As we will show, modeling leakage in a contract becomes as easy as adding few `leak` statements to one of the many existing SAIL models for RISC-V, ARM, etc. (GENOA supports all SAIL models), providing an interface to our tool and applying it to check for modeling gaps (more on this in Section 5). Parts of the IBEX contract are shown in Listings 1 to 6.

The SAIL manual [2] and the work of Armstrong et al. [4] provide in-depth explanations of the syntax, we give a brief overview. In Listing 1 we define the architectural state of a processor, consisting of 32-bit registers which are declared as global variables.
Listing 1: Contract model of state defined in Genoa.

```plaintext
// adopted from RISCV Sail Model, see license in Listing 6
register PC : bits(32)
register nextPC : bits(32)
register x1 : bits(32) ...
register rf_pa : bits(32) // register file read port A
register rf_pb : bits(32) // register file read port B
register mem_last_addr : bits(32) // address of last access
register mem_last_read : bits(32) // data from last instr.
register mem_last_addr : bits(32) // data from last instr.

// adopted from RISCV Sail Model, see license in Listing 6
// shadow registers
register nextPC : bits(32)
register mem_last_read : bits(32)

Additional shadow registers are introduced to model leakage which arises from microarchitectural state in hardware. For example, rf_pa is used to remember the value last read from the register file but is not used in the specification of instruction semantics. Its value is maintained in the model and later on leaked in `leak` statements to model leakage of instructions accessing the register file since such leakage involves the value of the register read last [45]. Every contract must specify a function step defining how a single instruction is executed. For IBEX, `step_ibex` shown in Listing 2 decodes the machine code instruction (`encdec`) provided as parameter `op` and returns whether the instruction executes (`execute`) successfully. Both `encdec` and `execute` are scattered into multiple clauses which describe the decoding, respectively execution, for a few instructions loosely belonging to a category. Each category is represented by a datatype `ast`, e.g., `RTYPE` for instructions operating on three ISA registers, represented by three indices for destination and two operands, as well as another datatype `rop` for different operations. Listing 3 shows the model of `RTYPE` instructions; `encdec` maps between instruction bits and `ast` representations using conditional pattern matching. In line 6 `rs1` represents the index bits of the first source register. The instruction semantic and leakage is specified in `execute`, `X(rs1)` returns the value of the register addressed by `rs1`. Leakage which is common across multiple instruction categories is exposed with a call to function `common_leakage` (we defer the descriptions to Section 5.2, Listing 4). The semantics of the different operations (add, signed less than, etc.) is defined in the `match` statement. Function `overwrite_leakage` specifies transition leakage emitted while writing the result to the destination register. In summary, Genoa allows designers to quickly construct and adjust contracts, while the human-readable specification supports the systematic development of side-channel protected software.

3.2 Contract Formalization

In the previous section we explained how to express contracts in the Genoa DSL. We now describe Genoa’s profound formal semantics which is the basis for security verification and compliance checking.

Listing 2: Model of instruction-step \( \gamma \) defined in Genoa.

```plaintext
// adopted from RISCV Sail Model, see license in Listing 6
function step_ibex (op : bits(32)) -> bool = {
    nextPC = PC + 4;
    let instruction = encdec(op);
    tick_pc();
    match ret { RETIRE_SUCCESS => return true,
        RETIRE_FAIL => return false}}

The small-steps semantics of Genoa are defined as a reduction 

\[
(\delta, s, L) \mapsto (\delta', s', L').
\]

\( \delta \) is the context containing the definition of functions and the values of local and global variables, \( s \) is a sequence of statements and \( L \) is the leakage exposed during execution. After the execution of a Genoa statement (not to be confused with an instruction) \( \delta' \) is the resulting context, \( s' \) are the remaining statements and \( L' \supseteq L \) is the resulting leakage. Leakage cannot be erased. All statements except `leak` do not add leakage and their transformation rules stay the same as in SAIL [3]. A `leak` statement appends its operands \( v_i \), ..., \( v_n \) to the execution leakage (\( ; \) is a sequence of statements):

\[
(\delta, \text{leak}\{v_1, ..., v_n\}; s, L) \mapsto (\delta, s, L \cup \{v_1(\sigma')|...|v_n(\sigma')\}).
\]

A `leak` statement may expose multiple values, which allows abstracting away from particular assumptions such as Hamming-Distance leakage, as processors are allowed to leak any combination of the values exposed by a `leak`. While Genoa does not feature a construct to sample random values, sampling can be mimicked by reading from a dedicated state region containing randomness.

The behavior of a program is defined by user-supplied execution semantics which are specified in the contract. The contract specification written in Genoa thus defines the context \( \delta \) for small-step execution and, as for hardware, the contract state \( \sigma' \in \mathbb{P}^{\text{V}} \) denotes the values of variables \( \sigma' \in \mathcal{V} \), further on referred to as locations. Based on these definitions, we can now define the semantics for the execution of an entire instruction, denoted by the step function \( \chi \) starting in state \( \sigma_i \) and returning the state \( \sigma_i+1 \) and a set of side-channel leakages \( \mathcal{L}_i \) of executing the \( i \)-th instruction:

\[
\chi(\sigma_i) = (\sigma_{i+1}; \mathcal{L}_i).
\]
The instruction to be executed is determined by the state $\sigma_i^c$ itself, e.g., by the value of the program counter. The execution of an instruction corresponds to the many-steps evaluation of the instruction-steps function $\chi$ using the small-steps semantics described before. $\chi$ is part of the contract (for IBEX step, ibex) and supplied by the user; to simplify our tool state $\sigma_i^c$ is implicitly passed while the instruction to be executed is passed explicitly. A step can either fail or succeed, indicated by a Boolean flag. The criteria for failing the execution is governed by user-defined assumptions. For IBEX these prohibit illegal instructions, accesses of non-existent registers or unaligned memory accesses. In the following, we depict execution of an entire instruction in the contract with

$$
\sigma_i^c \xrightarrow{L^c_i} \sigma_{i+1}.
$$

Finally, we define the execution of programs in a contract. Contract $\langle P \rangle^c$, $\langle P \rangle^h$ models the execution of program $P$ starting in initial state $\sigma_0^c$ and resulting in state $\sigma_n^c$ while producing the accumulated observable side-channel information $L^c_n = \bigcup_{i=0}^{n-1} L^c_i$, i.e.,

$$
\langle P \rangle^c(\sigma_0^c) = (\sigma_n^c, L^c_n).
$$

### 3.3 Software Security

In this section we link security of abstract gadgets to the execution in a contract or on hardware, i.e., we define security w.r.t. the leakages specified in a contract or gate-level leakage of a processor.

Gadgets have as inputs and outputs either shares, random or public values, which are linked to the definition of Stateful $t$-(S)NI (Definition 3). However, when the implementation of a gadget is executed within a contract or hardware then the gadget’s inputs are located in the state $\sigma$ with an implementation-specific placement, e.g., shares could be in registers or memory. We introduce policies $\pi$ to translate between the structured in- and outputs of a gadget and the states in a contract, respectively hardware. Input policy $\pi_{in} : (X, r, p) \mapsto \sigma_0$ constructs a state given values of variables for input shares, random and public variables but also the converse; extracting the values of gadget inputs given a state. In practice, such a policy is an annotation which defines where shares, random and public (initial) values are located w.r.t. locations of the state. Similar, output policy $\pi_{out} : (y, o) \mapsto \sigma_n$ maps between the values of public outputs and output shares of a gadget and the state $\sigma_n$ resulting from an execution. Since Stateful $t$-(S)NI is defined for random variables let $\sigma$ denote the random variable for states. Using policies we can link Stateful $t$-(S)NI security of gadgets to the execution of their concrete implementation $P$ within big-steps semantics $\langle P \rangle$ representing either the contract or hardware:

**Definition 4** ($t$-(S)NI under $\langle P \rangle$). An implementation $P$ of gadget $G(X, r, p)$ is $t$-(S)NI secure w.r.t. semantic $\langle P \rangle$ and placement policies $\pi_{in}, \pi_{out}$ if the gadget $G’(X, r, p) = (y, o, L_{0,n})$ is $t$-(S)NI according to Definition 3, where the inputs of the gadget correspond to the starting states $\sigma_0 = \pi_{in}((X, r, p))$ while leakages and gadget outputs correspond to the random variables $\pi_{out}(y, o) = \sigma_n$ resulting from execution $\langle P \rangle(\sigma_0) = (\sigma_n, L_{0,n})$.

The actual verification of security for software implementations follows the same principles as outlined by Barbé et al. [9], which also describes representation of policies. However, the dependent

$$
\langle P \rangle^c(\sigma_0^c) : \sigma_0^c \xrightarrow{L^c_0} \sigma_1^c \xrightarrow{L^c_1} \ldots \xrightarrow{L^c_{n-1}} \sigma_n^c,
$$

$$
\langle P \rangle^h(\sigma_0^h) : \sigma_0^h \xrightarrow{L^h_0} \sigma_1^h \xrightarrow{L^h_1} \ldots \xrightarrow{L^h_{m-1}} \sigma_m^h.
$$

**Figure 1:** Compliance for a full program execution

The type system of Genoa enables new approaches to verification of masked conversion functions and arithmetic masking in rings with prime moduli for security orders $t > 1$. We leave the development of software verification tools to dedicated future work.

### 3.4 Hardware Compliance With a Contract

We now turn towards the question of model completeness and define compliance with a contract, a formal property expressing that the results and leakages from execution on a CPU are modeled by a contract according to Definition 2. This property is verified in Section 4 and ensures, as we prove in Section 3.5, that any program that is Stateful $t$-(S)NI secure in a contract mitigates all order-reducing leakage caused by the gate-level leakage of a processor.

A program $P$ executed in initial hardware state $\sigma_0^h$ leads to leakages $L_{0,m}^h$ and final state $\sigma_m^h$ when executed on processor $\langle P \rangle^h$:

$$
\langle P \rangle^h(\sigma_0^h) = (\sigma_m^h, L_{0,m}^h).
$$

In contrast to contracts the execution proceeds in clock-cycles instead of instruction-steps, i.e., one step in hardware corresponds to one clock cycle as defined in Section 2.1:

$$
\sigma_j^h \xrightarrow{L^h_j} \sigma_{j+1}^h.
$$

Compliance expresses the property that all leakage and all outputs of hardware execution $\langle P \rangle^h$ can be modeled (according to Definition 2) from execution in a contract $\langle P \rangle^c$ as long as the starting states are similar, i.e., execute the same program under equivalent inputs, depicted in Figure 1.

In Definition 5 we introduce a Boolean relation between hardware state $\sigma^h$ and contract state $\sigma^c$ expressing that the values contained at a specific location $v^h$ in the hardware can be modeled from a location $v^c$ in the contract, e.g., register $x_1$ models its counterpart in hardware. Which contract locations model some hardware location is defined in the simulation mapping $M$ provided by users alongside every contract and checked by our tool. The mapping specifies for all registers in the hardware (including finite state machines, decode stages, etc.) a location in the contract modeling the hardware location. To ease notation assume there are contract locations $\sigma_0^c, \sigma_1^c \in V^c$ which are constant zero, respectively one, and later on used to express constraints on hardware execution.

**Definition 5** (Similar states: $\sigma^h \models M \sigma^c$). Two states $\sigma^h$ and $\sigma^c$, with respective locations $V^h$ and $V^c$ are similar under simulation mapping $M \subseteq V^h \times V^c$, written $\sigma^h \models M \sigma^c$, if and only if

$$
\bigwedge_{(v^h, v^c) \in M} v^h(\sigma^h) = v^c(\sigma^c).
$$

Simulation mapping $M$ is said to be complete if for all hardware locations $V^h$ a mapping is defined.
We now give the definition of compliance, ensuring that semantic and leakage of execution of hardware is correctly modeled:

**Definition 6 (Compliance: \(\llbracket P \rrbracket^h \circ M \llbracket L \rrbracket^h\)).** A hardware implementation is compliant with a contract under simulation mapping \(M\) if for every program \(P\) and starting hardware and contract states \(\sigma_0^h\) and \(\sigma_0^c\), the program executions

\[
\llbracket P \rrbracket^c (\sigma_0^c) = (\sigma_m^c, L_{0,m}^c) \quad \text{and} \quad \llbracket P \rrbracket^h (\sigma_0^h) = (\sigma_m^h, L_{0,m}^h)
\]

fulfill the following conditions:

1. **States remain similar:** Whenever \(\sigma_0^h\) and \(\sigma_0^c\) are similar under \(M\), so are resulting states \(\sigma_m^h\) and \(\sigma_m^c\):

   \[
   \forall \sigma_0^h, \sigma_0^c : \sigma_m^h \cong_M \sigma_m^c \Rightarrow \sigma_m^h \cong_M \sigma_m^c.
   \]

2. **Leaks are modeled:** For every leak \(\lambda_g (a^h_{i-1}, a^h_i) \in L_{0,m}^h\) observable in hardware, there exists a leak \(\lambda (\sigma_0^c) \in L_{0,c}^c\) in the contract and a function \(f_\lambda : \text{Dom}(\lambda) \rightarrow \text{Dom}(\lambda_g)\) that models \(\lambda_g\) from \(\lambda\) under relation \(\sigma_0^c \cong_M \sigma_0^c\) according to Definition 2:

   \[
   \forall \sigma_0^h, \sigma_0^c : \sigma_m^h \cong_M \sigma_m^c \Rightarrow f_\lambda \circ \lambda (\sigma_0^c) = \lambda_g (a^h_{i-1}, a^h_i).
   \]

The notion of similar states allows to express a key ingredient for the relational definition of compliance: if execution in a contract and hardware start in a similar state, then execution must end in similar states such that the hardware execution’s results can be modeled according to the simulation mapping (Clause 1 of Definition 6). Further, the second part of compliance expresses that every gate-level leak observable during execution in hardware must be modeled by a single, fixed leak observable during execution in the contract (Clause 2 of Definition 6). Combined, this guarantees that software which is Stateful \(t\)-(S)NI secure when executed in the contract, is necessarily Stateful \(t\)-(S)NI when executed on compliant hardware.

### 3.5 End-to-end security

It remains to prove our E2E security claim: any implementation \(P\) of gadget \(G\) that is Stateful \(t\)-(S)NI w.r.t. the leakages of a contract must be Stateful \(t\)-(S)NI w.r.t. all gate-level leakage when executed on any compliant hardware and as such its security order cannot be decreased by leakage of the processor. However, E2E security is claimed for the same software \(P\) implementing some gadget \(G\) and running on a processor and in the contract, i.e., both executions use the same structured inputs and outputs. Since the states in hardware and contract may have different structures we introduce a definition to ensure that the placement of inputs in hardware \(\pi_{in}^h \circ M\) is similar to the ones \(\pi_{in}^c, \pi_{out}^c\) for which \(t\)-(S)NI was shown in the contract. A hardware policy can be derived from a contract policy by substituting the locations which define where a value resides in the state according to the simulation mapping.

**Definition 7 (Similar Policy (\(\pi^h \cong_M \pi^c\))).** Let contract policy \(\pi^c : (d_1, \ldots, d_n) \mapsto \pi^c\) link sets of values \(d_1, \ldots, d_n\) to contract state \(\sigma^c\). Hardware policy \(\pi^h : (d_1, \ldots, d_n) \mapsto \pi^h\) is similar to \(\pi^c\), denoted \(\pi^h \cong_M \pi^c\) if any pair of contract and hardware states constructed from the same sets of values are similar under mapping \(M\):

\[
\forall \sigma^h = \pi^h (d_1, \ldots, d_n), \sigma^c = \pi^c (d_1, \ldots, d_n) : \sigma^h \cong_M \sigma^c.
\]

Instead of proving the security reduction for \(t\)-(S)NI directly we prove a general model reduction: any observations made by an adversary interacting with hardware may be modeled with a contract the hardware complies with instead. We emphasize the difference: \(t\)-(S)NI requires the existence of a simulation procedure whereas compliance guarantees the existence of a (stronger) modeling function easing the subsequent security reduction.

**Theorem 2 (Model Reduction).** Let \(P\) be a program, and the gadgets \(G^c (\mathcal{X}, r, p) = (\tilde{y}^c, \sigma^c, L^c_{0,n})\) and \(G^h (\mathcal{X}, r, p) = (\tilde{y}^h, \sigma^h, L^h_{0,m})\) correspond to the program executions \(\llbracket P \rrbracket^c (\sigma_0^c) = (\sigma_m^c, L_{0,m}^c)\), respectively \(\llbracket P \rrbracket^h (\sigma_0^h) = (\sigma_m^h, L_{0,m}^h)\), under policies \(\pi_{in}^c\) and \(\pi_{out}^c\), respectively \(\pi_{in}^h\) and \(\pi_{out}^h\), with \(\sigma_0^c = \pi_{in}^c (\mathcal{X}, r, p), \sigma_0^h = \pi_{in}^h (\mathcal{X}, r, p), \sigma_m^c = \pi_{out}^c (\tilde{y}^c, o^c), \text{and} \sigma_m^h = \pi_{out}^h (\tilde{y}^h, o^h).\) Furthermore, let \(\llbracket \bullet \rrbracket^h \circ_M \llbracket \bullet \rrbracket^c\) for \(\pi_{in}^c \cong_M \pi_{in}^h\) and \(\pi_{out}^c \cong_M \pi_{out}^h\) under complete mapping \(M\). For every set of observations in hardware on \(\tilde{y}^c\) or \(o^c\) there is an equally sized set of observations in the contract on \(\tilde{y}^c\) or \(o^c\) which allows to model the observations under the identity function:

\[
\forall o^h \subseteq \tilde{y}^h \exists \tilde{y}^c \subseteq \tilde{y}^c : o^h = o^c
\]

\[
\forall o^c \subseteq \tilde{y}^c \exists o^h \subseteq \tilde{y}^h : o^c = o^h.
\]

In addition, for every set of observations in hardware on \(L^h_{0,m}\), a modeling function \(T^L\) and a (potentially smaller) set of observations in the contract on \(L^c_{0,n}\) allow to model the observations in hardware:

\[
\forall e^c_L \subseteq L^c_{0,n} \exists e^h_L \subseteq L^h_{0,m} : e^c_L \subseteq T^L (e^h_L).
\]

**Proof.** The gadgets \(G^c\) and \(G^h\) operate on equally distributed inputs and the policies for hardware are similar, thus for every initial state \(\sigma_0^h\) there must be a starting state \(\sigma_0^c\) similar under mapping \(M\), i.e., \(\sigma_0^h \cong_M \sigma_0^c\). Since hardware is compliant with the contract, the resulting states are similar as well, i.e., \(\sigma_m^h \cong_M \sigma_m^c\) and since every observation in \(\sigma_0^h\), respectively \(\sigma_0^c\) is an observation on the value of a location in \(\sigma_0^m\), it follows directly that there exists a single location in the contract \(e_0^c\), respectively \(e_0^h\), according to the mapping \(M\) which models the observation, fulfilling (4) and (5). From Lemma 1 and Clause 2 of Definition 6 it follows that every observation \(\lambda (\sigma_0^h) \in e_0^h\) can be modeled from some contract leak \(\lambda (\sigma_0^c) \in L^c_{0,n}\) using \(f_\lambda\) as modeling function. Grouping the necessary \(\lambda (\sigma_0^c)\) as the set of random variables \(e_0^c\) results in \(e_0^c \subseteq e_0^h\) and defining \(T^L\) as the set of respective \(f_\lambda\) implies (6), completing the proof.

From Theorem 3, we derive simulatability of mixed observations in Corollary 3. Furthermore, the reduction from Stateful \(t\)-(S)NI in hardware to Stateful \(t\)-(S)NI in contract stated in Corollary 4 is a direct consequence of Theorem 3 and Corollary 3.

**Corollary 3 (Mixed observations).** Let the setting be as in Theorem 2. Every set of mixed observations on leakage and shared outputs \(e_{L,\tilde{y}} \subseteq L^h \cup \tilde{y}^h\), can be modeled from some an equally sized set \(e_{L,\tilde{y}} \subseteq L^c \cup \tilde{y}^c\) by some modeling function \(T^L\).
COROLLARY 4 (END-TO-END SECURITY). Let the setting be as in Theorem 2. If gadget $G^c$ is $t$-$(S)$NI then gadget $G^h$ is also $t$-$(S)$NI since there exist simulators $T - L \psi \circ S$ and $F$ which simulate the outputs of $G^h$ according to Definition 3.

This proof is valid for higher-order masking, i.e., $t \geq 1$, as each of the $t$ hardware observations in $e^h$ can be simulated from one observation in $e^c$ in the contract. The presented model reduction can be of help in proving the preservation of other security notions like PINI [12], threshold implementations [43] or probing security [31].

4 VERIFYING HARDWARE COMPLIANCE

Whereas Section 3 introduces contracts and what it means for hardware to be compliant, this section presents a method to actually check hardware compliance for a given processor, i.e., that the leakage of each of gate in the CPU netlist (i.e. the synthesized CPU design) and the semantic of instruction is correctly specified in the corresponding contract. The method is broken down into verification steps. Each step checks if the processor satisfies some part of Definition 6. First, we check whether similar hardware and contract states stay similar after executing an instruction according to Clause 1. Then, we check that each hardware leak can be modeled from a single leak emitted in the contract, according to Clause 2.

4.1 Verification Concept

In this section, we first suggest that it is possible to prove a processor compliant without looking at full program executions. We argue that looking at all possible single instruction executions is sufficient to form an inductive argument of compliance. Next, we give an overview of the individual verification steps needed to verify that a processor is compliant with a given contract. Finally, we present a method for indirectly proving the existence of modeling functions. This method is the backbone of the verification procedure and relies on encoding constraints into SMT formulas and checking their satisfiability with an SMT solver.

Single instructions. Checking compliance for all programs and pairs of processors and contracts using SMT solvers is computationally intractable. Instead we prove compliance inductively by showing that Definition 6 holds for all possible executions of a single instruction. Consequently, we require compliant processors to fulfill the outlined properties at the start and end of each instruction, as shown in Figure 2. Starting with similar states $\sigma^h_j$ and $\sigma^c_j$, the hardware executes $k$ cycle cycles and the contract executes one instruction step. The executions produce leaks $L^h_{j,k}$ and state $\sigma^h_{i+j}$, respectively $\sigma^c_{i+1}$, for which we need to show:

(a) States remain similar: The states $\sigma^h_{j,k}$ and $\sigma^c_{i+1}$ are similar under $M$ (marked red), i.e., every location in $\sigma^h_{j,k}$ is equal to the corresponding location in $\sigma^c_{i+1}$.

(b) Leaks are modeled: Every leak $\lambda^h_{j,k}(\sigma^h_{j,k}, \sigma^c_{i+1}) \in L^h_{j,k}$ produced by the processor (marked red) must be modeled by a single leak $\lambda(\sigma^c_j) \in L^c_i$ emitted in the contract execution.

These conditions are inductive and much stricter than the corresponding clauses in Definition 6, i.e., if the execution of a single instruction in an arbitrary valid starting state maintains the compliance properties, the processor complies with the contract for all possible program executions.

As seen in Figure 2, the hardware might require multiple clock cycles to execute an instruction while the contract always takes only one step. For the purposes of this paper, we define the starting point of an instruction as the moment it becomes in-flight, i.e., it reaches the decode stage, and its end point when it retires, i.e., the writeback completes. Therefore, we look at every possible instruction duration $k$ on that particular processor. Concurrent execution of instructions in the pipeline complicates this approach. For simple pipelines this is not an issue because the fetch stage does not operate with security-critical data, and the writeback stage can be made the synchronisation point for the induction, instead of its full re-tirement. In more complex pipelines, the methods described in this paper require checking leakage produced by hardware components directly influenced by the instruction bits.

Verifying that states remain similar. As the very first step in the verification procedure, we show that the hardware and contract states are similar throughout the whole execution. That is, we show that if the relation $\sigma^h_{j,k} \sim_M \sigma^c_{i+1}$ holds, the relation $\sigma^h_{j,k+1} \sim_M \sigma^c_{i+1}$ must hold after the execution of a $k$-cycle instruction i.e., $\sigma^h_{j,k+1} = \chi^k(\sigma^h_j)$ and $\sigma^c_{i+1} = \chi(\sigma^c_j)$, no matter what the starting states were. This is essentially a full-fledged functional equivalence proof between the hardware and the contract. If this check succeeds, we have shown that the processor satisfies Clause 1 of Definition 6 because $\sim_M$ is conserved over the execution of an instruction. Section 4.3 formalizes the verification step and gives a verification method.

Finding modeling functions for gates. Before verifying that leaks are modeled, we require an intermediate verification step that provides information about the old values of gates. This constrains the old values of each gate $g$, therefore implicitly constraining the possible values of the corresponding leak $\lambda_g$. Otherwise, the old value could directly leak secrets, trivially breaking leakage modeling. For every gate $g \in G$ in the hardware, we show that $g$ can be modeled by some function $f_g : B^n \rightarrow B^m$ that only uses a (small) subset of contract state bits $\theta_g : B^{V^q} \rightarrow B^m$, i.e.,

$$\exists f_g : \forall \sigma^h_j, \sigma^c_j : \sigma^h_j \sim_M \sigma^c_j \Rightarrow f_g \circ \theta_g \circ \chi(\sigma^c_j) = g \circ \chi^{k-1}(\sigma^h_j). \ (7)$$

Ideally, we want to prove the existence of a modeling function that uses as little contract state information $\theta_g$ as possible. Section 4.4 gives exact definitions of the verification checks and the greedy minimization procedure for $\theta_g$.

Verifying that leaks are modeled. In this verification step, we check whether the hardware leakage is properly modeled from contract leakage for any possible instruction execution, starting in any pair of similar states $\sigma^h_j \sim_M \sigma^c_j$. If the check succeeds, the proper modeling throughout any program execution is implied by
We see that if all three premises are fulfilled simultaneously, then $f$ contains information about both the old and the new values of gate $g$ for any clock cycle $l$ of the executed instruction. We analyze each hardware leak function $\lambda_g$ separately by going through all leakage functions $\lambda : \mathbb{B}^{\mathbb{W}^1} \to \mathbb{B}^2$ and checking if there is a function $f_{\lambda} : \mathbb{B}^m \to \mathbb{B}^2$ that models $\lambda_g$ from $\lambda$, whenever states $\sigma^h_i$ and $\sigma^c_i$ are similar, the contract leak is emmitted, i.e., $\lambda(\sigma^c_i) \in L_f^c$, and $f_{\lambda}$ models the previous value of the gate $g$ from $\sigma_g$. Written formally:

$$\forall \sigma^h_i, \sigma^c_i : \sigma^h_i \approx_M \sigma^c_i \land f_{\lambda} \circ \theta_g \circ \chi(\sigma^c_i) = g \circ \chi^{-1}(\sigma^h_i) \land \lambda(\sigma^c_i) \in L^c_f \Rightarrow f_{\lambda} \circ \lambda(\sigma^c_i) = \lambda_g(\sigma^c_{i+1}, \sigma^h_{i+1})$$

(8)

Additionally, we require that for any possible state $\sigma^c_i$ at least one leak $f_{\lambda}$ fulfills (8), guaranteeing that Clause 2 of the compliance definition is fulfilled. Section 4.5 gives a more detailed description.

**Existence of modeling functions.** Within the last two verification steps, we check that functions over the hardware state $\sigma^h$ can be modeled from functions over the contract state $\sigma^c$ whenever $\sigma^h \approx_M \sigma^c$. This involves proving the existence of modeling functions from Definition 2. However, automatically finding modeling functions is intractable in general [21]. We circumvent this issue by proving the existence of modeling functions without finding their definitions. Theorem 5 presents the condition we need to check.

**Theorem 5 (Existence of Modeling Function).** There exists a modeling function $f : U \to V$ according to Def. 2 if and only if

$$\forall h', h, c, c' \in C : \Psi(h, c) \land \Psi(h', c') \land f_{\lambda}(c) = f_{\lambda}(c') \Rightarrow f_{\lambda}(h) = f_{\lambda}(h')$$

(9)

Proof. We prove the equality of the two statements by showing an implication in both directions. First, we prove that (9) follows from (1). From the functional congruence of $f$, we have:

$$\forall c, c' \in C : f_{\lambda}(c) = f_{\lambda}(c') \Rightarrow (f \circ f_{\lambda}(c) = f \circ f_{\lambda}(c'))$$

After instantiating the statement (1) separately for the primed and non-primed versions of $h \in H$ and $c \in C$, we get:

$$\forall h \in H, c \in C : \Psi(h, c) \Rightarrow f \circ f_{\lambda}(c) = f_{\lambda}(h)$$

$$\forall h' \in H, c \in C : \Psi(h', c) \Rightarrow f \circ f_{\lambda}(c') = f_{\lambda}(h')$$

We see that if all three premises are fulfilled simultaneously, then also all consequences of the implication must be fulfilled simultaneously. Therefore, we consolidate the left- and right-hand sides. Afterwards, we simplify the right-hand side by substituting $f \circ f_{\lambda}(c)$ with $f_{\lambda}(h)$, and respectively $f \circ f_{\lambda}(c')$ with $f_{\lambda}(h')$, to get (9).

For the second direction of the proof, we assume (9) and construct $f$ so that it fulfills (1) and is well defined for all $u \in U$. First, we define the subset $U \subseteq U$ of function inputs as

$$\bar{U} := \{u \mid \exists h \in H, c \in C : u = f_{\lambda}(c) \land \Psi(h, c)\}$$

(10)

For inputs $u \in U', \bar{U}$, we define $f(u)$ as an arbitrary result $v \in V$. This partial definition trivially fulfills (1). For all other $u \in \bar{U}$, we define $f(u) := f_{\lambda}(h)$, for an arbitrary qualified $h$ and $c$ as in (10).

We now argue that this portion of $f$ is well defined, because $f_{\lambda}(h)$ is fixed for $u$. Consider the case where we can pick two such pairs:

$$\exists h, h' \in H, c, c' \in C : u = f_{\lambda}(c) \land \Psi(h, c) \land u = f_{\lambda}(c') \land \Psi(h', c')$$

Because $f_{\lambda}(c) = f_{\lambda}(c') = u$, assumption (9) implies that $f_{\lambda}(h)$ is unique since we always get $f_{\lambda}(h') = f_{\lambda}(h)$. $\square$

The underlying principle behind Theorem 5 can be thought of as partial functional congruence. Plainly speaking, if equal inputs $f_{\lambda}(c)$ and $f_{\lambda}(c')$ always result in equal outputs $f_{\lambda}(h)$ and $f_{\lambda}(h')$, then there must also be a function mapping between them. Moreover, Theorem 5 can be translated into the quantifier-free SMT fragment and efficiently checked with modern SMT solvers.

### 4.2 Verification Prerequisites

Real program execution within a processor is subject to many internal assumptions and restrictions that need to be considered when checking the compliance properties. In particular, we define normal operating conditions for the execution of an instruction, as well as constraints related to the mapping $M$ from Section 3.4.

**Normal operating conditions.** The hardware of a processor has many input ports and internal registers that are invisible to a software developer and are subject to hidden assumptions under normal operating conditions. In this section, we introduce predicates $\phi^h$ to explicitly represent these assumptions. We use the predicate $\phi^h_{\text{dev}}(\sigma^h)$ to represent the usual assumptions a software developer might have, such as the processor not getting reset, triggering an interrupt, going into debug mode, or getting memory access errors. Similarly, there are several internal conditions for the processor to fetch, start the execution of, and retire an instruction. We formalize these conditions as $\phi^h_{\text{inst}}(\sigma^h)$, $0 \leq l < k$ for the $l$-th cycle in $k$-cycle instructions and apply them for the intermediate states $\sigma^h_{i-1} = (\sigma^h_l)_{l=0}^{k-1}$. Sometimes, a contract is not able to execute an instruction because it violates some sanity conditions such as the instruction not being implemented or triggering a fault. We formalize the condition of the contract successfully retiring an instruction as $\phi^h_{\text{ret}}(\sigma^h)$. We aggregate these conditions into $\phi^h_{\text{noc}}$ as

$$\phi^h_{\text{noc}}(\sigma^h, \sigma^c) := \phi^h_{\text{ret}}(\sigma^h) \land \bigwedge_{l=0}^{k-1} \phi^h_{\text{dev}}(\sigma^h_{i+1}) \land \phi^h_{\text{inst}}(\sigma^h_{i+1})$$

There are also some constraints that concern multiple executions of the hardware and contract. For such predicates we write $\phi^c$ instead. We define $\phi^c_{\text{ports}}(\sigma^h, \sigma^h)$ as the constraint that certain processor input ports only contain public values. More concretely, for two executions of the hardware, these input ports are required to produce identical values. There are also similar execution-spanning conditions for the contract. For instance, the contract should forbid the program counter from becoming secret dependent. The predicate $\phi^c_{\text{ret}}(\sigma^h, \sigma^c)$ expresses these constraints, and is stricter than both $\phi^c_{\text{ret}}(\sigma^c)$ and $\phi^c_{\text{ret}}(\sigma^c)$ separately. Finally, we extend $\phi^h_{\text{noc}}$ to...
we also require a predicate expressing that all registers, which are verification targets require this as an assumption. We check the property is inductive, and we use it in all further checks.

Example to the state similarity property of Definition 6. Otherwise, we use an SMT solver to check for states that satisfy both \( \phi \) implies the first hardware compliance condition (Clause 1) from Definition 4.3 Verifying that States Remain Similar

As introduced in Section 3.4, hardware and contract states can be similar under a mapping. For expressing that two states \( \alpha^h \) and \( \alpha^c \) are similar under mapping \( M \), we use the predicate \( \phi^h \) as defined in (3). Conversely, we also require a predicate expressing that all registers, which are not in the mapping \( M \), are equivalent across hardware executions of the same program. We specify this property of two hardware states \( \alpha^h \) and \( \alpha^M \) for the mapping \( M \) and locations \( V^h \) as

\[
\phi^M (\alpha^h, \alpha^M) := \bigwedge_{v^h \in V^h} \bigwedge_{(\sigma^h, \sigma^c) \in M} \phi^h (\alpha^h, \alpha^c).
\]

4.3 Verifying that States Remain Similar

As introduced in Section 4.1, we verify that the hardware and contract states resulting from the execution of a program are similar by checking the equivalence of the states. We require that the states \( \alpha^h \) and \( \alpha^c \) exist at the start of the instruction, prove that the states \( \alpha^h_{j+k} \) and \( \alpha^c_{j+k} \) are similar after the \( k \)-cycle instruction terminates. This is a straightforward functional equivalence check under the assumption that \( \phi^h \) holds.

**Proposition 1.** Let \( \alpha^h \) be a hardware state and \( \alpha^c \) be the corresponding contract state under mapping \( M \). Furthermore, let \( \alpha^h_{j+k} = \chi^h (\alpha^c_j) \) and \( \alpha^c_{j+k+1} = \chi (\alpha^c_j) \) be the hardware state and contract state after the execution of the instruction. Inductively,

\[
\exists \sigma^h_{j+k}, \sigma^c_j : \phi^h (\sigma^h_{j+k}, \sigma^c_j) \wedge \phi^M (\sigma^h_{j+k}, \sigma^c_j) \wedge \neg \phi^M (\sigma^h_{j+k+1}, \sigma^c_{j+k+1}).
\] (11)

implies the first hardware compliance condition (Clause 1) from Definition 6 under normal operating conditions.

Proposition 1 specifies how exactly this check is performed. We use an SMT solver to check for states that satisfy both \( \phi^h \) and \( \phi^M \), but their successors break \( \phi^M \). Any such case is a counterexample to the state similarity property of Definition 6. Otherwise the property is inductive, and we use it in all further checks.

We also check that \( \phi^M \) is inductive because all of the further verification targets require this as an assumption. We check the inductiveness by asking an SMT solver

\[
\exists \sigma^h_j, \sigma^c_j : \phi^h (\sigma^h_j, \sigma^c_j) \wedge \phi^M (\sigma^h_j, \sigma^c_j) \wedge \phi^M (\sigma^h_{j+k}, \sigma^c_{j+k}).
\] (12)

4.4 Finding Modeling Functions for Gates

In this section, we introduce a method that finds a small number of contract registers from which the value of a hardware gate is modeled. This intermediate step determines, and later on restricts, the values a gate can have at the end of the previous instruction. Corollary 6 instantiates Theorem 5 under normal operating conditions and presents a method for checking whether the value of a hardware gate can be modeled by contract state bits \( \theta_g \).

**Corollary 6.** Let \( \alpha^h \) be a hardware state and \( \alpha^c \) the corresponding contract state under mapping \( M \) that fulfill both (11) and (12).

Furthermore, let \( \alpha^h_{j+k-1} = \chi^h (\alpha^c_{j+k-1}) \) be the last hardware state before the instruction terminates, and \( \alpha^c_{j+k} = \chi (\alpha^c_{j+k}) \) be the contract state after the instruction terminates. The contract function \( \theta_g \) models gate \( g \) in cycle \( k-1 \) under normal operating conditions if and only if

\[
\exists \sigma^h_j, \sigma^c_j : \phi^h (\sigma^h_j, \sigma^c_j) \wedge \phi^M (\sigma^h_j, \sigma^c_j) \wedge \phi^M (\sigma^h_{j+k-1}, \sigma^c_{j+k-1}) \wedge \phi^M (\sigma^h_{j+k}, \sigma^c_{j+k})
\]

implies (13) which says

\[
\theta_g (\sigma^c_j) = \theta_g (\sigma^c_{j+k-1}) \wedge g (\sigma^h_{j+k-1}) \neq g (\sigma^h_{j+k}).
\]

Corollary 6 instantiates Theorem 5 under assumption of \( \phi^h \) and \( \phi^M \). Here, \( g \) is the function \( f_{ht} \) to be modeled, \( \theta_g \) is the function \( f_{fc} \) whose results are used as inputs for the modeling function, and \( \phi^M \) is the relation \( \Psi \) between the hardware and contract states.

However, not all functions \( \theta_g \) are useful, so we use a function like \( \theta_g (\sigma^c) = \sigma^c \) which can be modeled by the contract state. Instead, we propose the greedy minimization procedure shown in Algorithm 1. Here, we first check whether the hardware gate \( g \) can be modeled from the complete contract state. If this fails the contract does not model the hardware properly and the verification fails. Algorithm 1 iterates over all locations \( \sigma^c \) in the contract state and checks whether they are needed for modeling \( g \). In case they are not, i.e., formula (13) is unsatisfiable, they are removed from \( \theta_g \).

At the end, we have a (locally) minimal \( \theta_g \), where removing any component breaks the modeling of gate \( g \).

4.5 Verifying that Leaks Are Modeled

Lastly, we verify that the hardware leakage produced during the execution of an instruction can be modeled by the contract leakage.
emitted during the execution of the same instruction. The set of transition leaks produced in the hardware, starting in state \( \sigma^h_j \) and executing a \( k \)-cycle instruction is given by

\[
L^h_j, k = \left\{ \lambda g \left( \sigma^h_{j+1}, \sigma^h_{j+k} \right) | g \in G, 0 \leq l < k \right\}.
\]

As established in Section 4.1, we analyze every hardware leak \( \lambda g \left( \sigma^h_{j+1}, \sigma^h_{j+k} \right) \) separately and show that there is a set of leak statements \( L^h \subseteq L^h_j \) such that every \( \lambda g \) can be modeled by \( \lambda (\sigma^h_j) \in L^h \). Whenever the corresponding leak statement is reached in the contract, written as \( \phi^\text{emit}(\sigma^h_j, \lambda) \). Here, we use the intermediate proof of \( \lambda (\sigma^h_j) \) being modeled by \( \phi^\text{emit}(\sigma^h_j, \lambda) \) from Corollary 6.

**Proposition 2.** Let \( \sigma^h_j \) be the predecessor of hardware state \( \sigma^h_j = \chi(\sigma^h_{j-1}) \), and \( \sigma^h_j \) be similar to contract state \( \sigma^c_j \) under mapping \( M \), fulfilling both (11) and (12). Furthermore, let \( \sigma^h_j \) = \( \chi(\sigma^h_j) \) with \( 0 \leq l < k \) be the hardware states reached throughout the execution of a \( k \)-cycle instruction. Let \( \lambda g \) be the leakage function of a hardware gate \( g \), and \( \phi^\text{emit}(\sigma^h_j, \lambda) \) be a contract function such that (13) holds. Crucially, let \( L^h \subseteq L^h_j \) be a set of contract leaks, such that for every \( \lambda (\sigma^h_j) \in L^h \):

\[
\begin{align*}
&\lambda g \left( \sigma^h_j, \sigma^h_{j-1}, \sigma^c_j, \sigma^c_{j-1} \right) \cdot \phi^\text{nec} \left( \sigma^h_j, \sigma^h_{j-1}, \sigma^c_j, \sigma^c_{j-1} \right) \cdot \phi^\text{emit} \left( \sigma^c_j, \lambda \right) \\
&\lambda (\sigma^h_j) \cdot \lambda g \left( \sigma^h_{j+1}, \sigma^h_{j+k-1}, \sigma^h_{j+k} \right) = \lambda g \left( \sigma^h_{j-1}, \sigma^h_{j+k-1} \right) = \lambda g \left( \sigma^h_{j+k-1}, \sigma^h_{j+k} \right) \\
&\lambda (\sigma^c_j) = \lambda (\sigma^c_{j-1}) \cdot \lambda g \left( \sigma^h_{j+1}, \sigma^h_{j+k} \right) = \lambda g \left( \sigma^h_{j+1}, \sigma^h_{j+k} \right) \neq \lambda g \left( \sigma^h_{j-1}, \sigma^h_{j+k-1} \right).
\end{align*}
\]

The leak function \( \lambda g \) in cycle \( l \) of a \( k \)-cycle instruction is modeled by a single contract leak function \( \lambda \) under relation \( \phi^M_{\text{rel}} \) and normal operating conditions \( \phi^\text{nec} \), according to Definition 6 if

\[
\forall \sigma^c_j, \sigma^c_{j-1} : \phi^\text{nec} \left( \sigma^h_j, \sigma^h_{j-1}, \sigma^c_j, \sigma^c_{j-1} \right) \land \phi^\text{rel} \left( \sigma^h_j, \sigma^h_{j-1}, \sigma^c_j, \sigma^c_{j-1} \right) \Rightarrow \lambda (\sigma^c_j) \in L^h.
\]

Again, the method outlined in Proposition 2 uses an SMT solver to show that the hardware cannot leak more information than the contract. If the solver is able to find a pair of states \( \sigma^h_j, \sigma^c_j \) for which the check fails, it has found a counterexample and the hardware does not comply with the leakage specified in the contract.

4.6 Modeling and Implementation

In this section, we briefly discuss the implementation and modeling details enabling our verification method. In particular, we discuss how all the formulas given to the SMT solver are constructed. The translation of a contract to a SMT formula is based on an existing \textit{Sail} back-end which allows to generate SMT formulas for custom predicates. However, the back-end cannot handle \textit{leak} statements. We perform two code-rewriting passes from \textit{Genoa} to \textit{Sail}. The first adds global state for each value in a \textit{leak} statement and replaces the \textit{leak} by an assignment to the respective global state. This reduces the \textit{Genoa} DSL to the \textit{Sail} subset supported by the SMT back-end. The second pass duplicates the variables representing contract state \( \sigma^c \) and leakages into prime and non-primed variants and duplicates the instruction-step function \( \chi \) by rewriting it to operate on either \( \sigma^c \) or \( \sigma^c' \) and resulting in \( \sigma^{c+1} \), respectively \( \sigma^{c+1'} \). Finally, \textit{Genoa} ensures that the initial and final states are preserved by the SMT back-end and asserts that the predicates \( \phi_{\text{ret}}, \phi_{\text{set}} \) and \( \phi_{\text{emit}} \) hold. Our tool receives the resulting SMT code as input.

**Gluing it all together.** Configuration files play a central role in the generation of formulas. In particular, our verification procedure expects an input where all of the hardware locations are declared, and either mapped onto contract registers with \( \phi^M_{\text{rel}} \) subject to developer assumptions \( \phi^M_{\text{dev}} \), port restrictions \( \phi^M_{\text{ports}} \), or instruction execution constraints \( \phi^M_{\text{instr}} \). Everything specified in the configuration is heavily sanity-checked, making sure that execution works properly, public signals \( \phi^M_{\text{pub}} \) remain public, and every hardware location is declared. Similarly, intermediate results such as \( \phi_{\text{dev}} \) are cached in configuration files and checked upon use. The \textit{IBEX} configuration is provided in Listing 7.

5 VERIFICATION PROCESS

We apply the verification method presented to the \textit{IBEX} processor and detail the process and results. \textit{IBEX} is an open source RISC-V processor that supports the \textit{Integer}, \textit{Embedded}, \textit{Multiplication}, \textit{Compressed} and \textit{Bit} manipulation ISA extensions [34]. For the purpose of our paper, we mainly target the \textit{E} extension, although adding support for the others is possible. The \textit{IBEX} pipeline consists of two stages, Instruction Fetch (IF) and Instruction Decode/Execute (ID/EX). Computations take place in the ID/EX stage, which consists of a decoder, a controller, and the register file, which forward the data into the arithmetic-logic unit (ALU) and the load-store unit (LSU). The outputs of the ALU and LSU are routed to the write-back logic (WBL), that decides which data is written into the register file. In the same pipeline stage, and hence in the same clock cycle, the result is written back into the register file.

The verification requires two manual and four automated steps:

1. Configuration of the processor by defining constraints
2. Definition of a mapping between hardware and contract
3. Automated sanity-check to ensure instructions defined in the contract can still execute in the processor under constraints
4. Automated check of similarity for resulting states (Section 4.3)
5. Automated check for gate modeling functions (Section 4.4)
6. Automated check for leakage modeling functions (Section 4.5)

In case any of the steps fail, the verification framework produces a detailed counterexample explaining the verification failure. The
We have proven that we align the contract and the hardware by restricting the state data_rvalid_i with previous outputs of the register file (modeled in leakage states file. Transitions in the first and second operand of instructions are caused these combinations. The WBL causes additional combinations: ALU or branch instructions after a memory load cause a transition between their results.

This common leakage covers leak effects previously discussed in related works. It models transition leakage produced in the ALU and WB stage, whose source are the two read ports of the register file. Transitions in the first and second operand of instructions are well-known [38, 39]. Interestingly, prior empirical analysis of the ARM M0 [39], a processor in the same performance and size class as IBEX, did not report interactions between the data loaded in the previous instruction and the current or past ALU operands.

Furthermore, the leakage is even caused by instructions which have no register operands like LUI (load unsigned immediate). The root cause of this effect is that the register file always decodes specific instruction bits as register addresses and forwards their contents to the ALU. In the case of LUI, these bits are actually part of the immediate value. This effect was observed by Gigerl et al. [25] but we characterize and describe the behavior more accurately. Prior analyses of the ARM M0 did not report similar effects [39], and instead reports that instructions with an immediate field behave as if they have only one operand which could be to the microarchitecture of the CPU or gaps in the empirical modeling procedure.

The leakage of load instructions modeled by load_leakage (Listing 5) differs from all other instructions. Here, the leak statement in common_leakage can be broken down into smaller leak statements. First off, because the ALU is always active, the current and previous values of the register file outputs are combined in line 9. Line 10 specifies leakage inherited from the prior instruction’s WBL through transition leakage. In contrast to prior work [25, 43], consecutive load instructions do not cause transition leakage between the loaded data because the contract disallows misaligned memory accesses. Similarly, IBEX does not expose transition leakage in subsequent memory writes, unlike several ARM architectures [9, 38]. This is likely because IBEX does not have additional registers in the memory path like other processors. However, IBEX does produce transition leakage between memory access addresses of loads and stores separated by an arbitrary amount of other instructions, as shown in line 11. IBEX causes this leakage because it always stores the last address for error-handling purposes.

We emphasize that the contract is provably complete for branching instructions; the behavior of these central instructions was so far not characterized.

5.3 Discussion
Performance. Verifying that a CPU design complies with a contract is computationally intensive, but can be well parallelized. We
ran the full verification on an Intel Xeon E5-4669 CPU with 88 logical cores running at 2.20GHz. The most time-consuming verification task is the search for gate modeling functions, which takes about 30.6 hours. This step is done once and then cached, and any changes to leak statements in the contract do not require it to be run again. Verifying the leakage modeling requires another 4.9 hours.

**Adaptability and scalability.** While we demonstrate our approach on the RISC-V IBEX core we emphasize that it is neither limited to RISC-V processors, nor the IBEX core. Verifying contract compliance for similar architectures and processors requires adapting the tool to their pipeline and properly configuring the verification procedure. We believe that the effort of including other architectures or processors mainly comes from adapting a contract to their CPU pipeline and properly configuring the verification. In any case, this effort is only required once per CPU netlist, and can be made either by the CPU designers themselves, or by any other person in case the CPU netlist is not IP restricted. Anybody with access to the contract can then verify masked software against it, without the need of having access to the CPU netlist itself.

**Hardware constraints and shortcomings.** We currently limit the scope of our contracts, and thus also the scope of masking verification, to the CPU core itself. Clearly, there may also be some other components that could cause power side-channel leaks during the execution of masked software. For example, RAM or data caches are another location where unintentional combinations of shares could occur. Within our framework, the leakage of such components would need to be verified separately and modeled within the CPU contract. Additionally, there are also cases when no “good” contract can be written for a CPU. One such example would be CPUs where the register file output is computed with a multiplexer tree, and would lead to a leak statement containing the whole register file.

So far, we analyze an instruction starting with the decode stage, which assumes that the fetch stage does not expose leakage depending on the fetched instruction. From what we have seen in IBEX and other processors, there is no leakage in the fetch stage that depends on the bits of the fetched instruction. For a similar reason, speculation or (secret-dependent) branch prediction is not a primary concern for our current analysis since these are usually not present in embedded devices.

**Masking verification.** Our tool currently focuses on value leakage and transition leakage, while our theoretical framework supports arbitrary gate-level leakage. Extending our verification tool to include further effects such as glitches makes an interesting future research question, and could be achieved by extending the encoding of leakage from Section 4.5. Our verification methodology and the contracts themselves support bitsliced and n-sliced masking [11], which are among the most popular implementation techniques for masked software. Our analysis, as well as prior work by others, observes joint leakage of bits stored in the same 32-bit register [22, 25, 39], rendering exotic concepts like share-slicing inherently insecure.

### 6 APPLICATION AND VALIDATION

We implement higher-order masked gadgets in software and verify their security against the IBEX contract. We demonstrate the benefit of contracts and validate our methodology by repeating the verification with an independent tool that directly verifies programs against the processor netlist and all of its side-effects. Finally, we assess the precision of contracts by confirming that the abstract leakage specification does not demand needless protection.

**Validation of the methodology and tool.** We port multiple second-order masked gadgets presented by Barthe et al. [9] to RISC-V and check their security (software compliance) using scVerif. For this, we perform a manual translation (which could be automated) of the GENOA contract to the DSL of scVerif and adopt its front-end slightly to accept RISC-V assembly. The resulting tool allows to prove software compliance (Definition 4), as well as the weaker notion of probing security for assembly implementations against the IBEX contract. There are no software masking verifiers capable of verifying t-(S)NI while also accounting for the CPU netlists. Therefore, we compare our results against Coco [25], a tool that accounts for the CPU netlist, but only supports probing security.

All gadgets are hardened by adding the least amount of clearing instructions until they are threshold probing secure, i.e., compliant with the contract under a weaker notion of security yet claimed secure against all gate-level leakage of IBEX. We have checked each gadget with both Coco and scVerif, and the results are shown in Table 1. The correctness of our methodology, hardware compliance checking tool and pen-and-paper model reduction (Theorem 2) are confirmed since there is no case where scVerif reports security while Coco rejects it.

**Quality of contracts.** We check that, whenever one of the clearing instructions that mitigate contract leakage is removed, Coco also rejects the program due to some gate-level leakage in the CPU netlist. If Coco would report that an implementation with less clearings is still secure, it would mean that the leakage generalization in the contract was too broad and requires needless hardening of the program. In our tests, whenever we removed any of the 11 clearings from Table 1, Coco always reported some gate-level leakage that breaks probing security. This indicates that our contract does not cause wrong insecurity reports (false negatives).

### 7 CONCLUSION

We introduced a methodology for creating software leakage models and proving their completeness based on the netlist of a CPU. Our rigorous approach allows us to treat the model as contract between the software and the hardware which provably guarantees end-to-end security: any implementation secure w.r.t. a contract is also secure on any compliant processor for all leakages exposed.
at gate-level. Overall the result significantly improve the secure construction of hardened software implementations. Besides providing strong guarantees of side-channel resistance, easing the soft porting of programs to different CPUs and the most extensive modeling of different instructions’s side-channel leakage, we think our approach could be beneficial for other applications as well. In particular, it could be used for leakage estimators or statistical security evaluations that can be derived from the executable Genoa contracts.

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REFERENCES


Appendix

### 7.1 RISC-V Model for IBEX

The missing parts of our contract for IBEX are depicted in Listing 6.

Listing 6: Contract model of remaining instructions for IBEX.

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**[43]** Copyright (c) 2017–2021 Prashanth Mundkur, Rishiyur S. Nikhil and Bluespec Inc., Jon French, Brian Campbell, Robert Norton-Wright, Alasdair Armstrong, Thomas Bauereiss, Shaked Flur, Christopher Pulte, Peter Sewell, Alexander Richardson, Hesham Almatary, Jessica Clarke, Microsoft, for contributions by Robert Norton-Wright and Nathaniel Wesley Filardo, Peter Rugg and Aril Computer Corp., for contributions by Scott Johnson */

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**[46]** This software was developed by SRI International and the 🅴撂 University of Cambridge Computer Laboratory ( Department of Computer Science and Technology ) under DARPA/AFFR contract FA8650-18-C-7809 ("CIFV"), and under DARPA contract HR0011-18-C-0016 ("ECATS") as part of the DARPA SSSI research programme. */

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**[48]** This work was supported by the Austrian Research Promotion Agency (FFG) through the FERMIOn project (grant number 867542). */
let x7_n = if (dest_idx == 0b00111) then {res} else {x7} in leak(x7, x7_n);
let x8_n = if (dest_idx == 0b00100) then {res} else {x8} in leak(x8, x8_n);
let x9_n = if (dest_idx == 0b00101) then {res} else {x9} in leak(x9, x9_n);
let x10_n = if (dest_idx == 0b00110) then {res} else {x10} in leak(x10, x10_n);
let x11_n = if (dest_idx == 0b01011) then {res} else {x11} in leak(x11, x11_n);
let x12_n = if (dest_idx == 0b01100) then {res} else {x12} in leak(x12, x12_n);
let x13_n = if (dest_idx == 0b01101) then {res} else {x13} in leak(x13, x13_n);
let x14_n = if (dest_idx == 0b01110) then {res} else {x14} in leak(x14, x14_n);
let x15_n = if (dest_idx == 0b01111) then {res} else {x15} in leak(x15, x15_n);

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THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT
LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR
OTHERWISE) ARISING IN ANY WAY OUT OF THE USE OF
THIS SOFTWARE, EVEN IF ADVISED OF THE POSSIBILITY
OF SUCH DAMAGE. */

val overwrite_leakage : (regidx, xlenbits) -> unit effect {->
let ret : xlenbits = match op {
let rs1_val = X(0b0 @ imm[6 .. 3]);
let rs2_val = X(0b0 @ imm[11 .. 8]);
let mem_last_read = 0x00000000;

function clause execute UTYPE(imm, rd, op) = {
let ret : xlenbits = EXTS(imm @ 0x0000);
let ret : xlenbits = match op {
RISCV_JAL => RISCV_JAL : (bits(21), regidx)

function overwrite_leakage(dest_idx : regidx, res : xlenbits
-> unit effect {->
let x7_n = if (dest_idx == 0b00111) then {res} else {x7} in leak(x7, x7_n);
let x8_n = if (dest_idx == 0b00100) then {res} else {x8} in leak(x8, x8_n);
let x9_n = if (dest_idx == 0b00101) then {res} else {x9} in leak(x9, x9_n);
let x10_n = if (dest_idx == 0b00110) then {res} else {x10} in leak(x10, x10_n);
let x11_n = if (dest_idx == 0b01011) then {res} else {x11} in leak(x11, x11_n);
let x12_n = if (dest_idx == 0b01100) then {res} else {x12} in leak(x12, x12_n);
let x13_n = if (dest_idx == 0b01101) then {res} else {x13} in leak(x13, x13_n);
let x14_n = if (dest_idx == 0b01110) then {res} else {x14} in leak(x14, x14_n);
let x15_n = if (dest_idx == 0b01111) then {res} else {x15} in leak(x15, x15_n);
}

/*********************/

val common_leakage : (xlenbits, xlenbits) -> unit effect {->

function clause execute UTYPE(imm, rd, op) = {
let ret : xlenbits = EXTS(imm @ 0x0000);
let ret : xlenbits = match op {
RISCV_JAL => RISCV_JAL : (bits(21), regidx)
function clause execute (RISCV_JAL(imm, rd)) = {
    let rs1_val = X(0b0 @ imm[18 .. 15]);
    let rs2_val = X(0b0 @ imm[3 .. 1] @ subrange_bits(imm, 11, 11));
    common_leakage(rs1_val, rs2_val);
    let t : xlenbits = PC + EXTS(imm);
    let rd_next = get_next_pc();
    overwrite_leakage(rd, rd_next);
    X(rd) = rd_next;
    if t[1 .. 0] == 0b00 then {
        set_next_pc(t);
        RETIRE_SUCCESS
    } else RETIRE_FAIL
}

/* **************************** */
union clause ast =
RISCV_JALR : (bits(12), regidx, regidx)

mapping clause encdec = RISCV_JALR(imm, rd)
<= imm @ rs1 @ 0b000 @ rd @ 0b110011
  function clause execute (RISCV_JALR(imm, rs1, rd)) = {
    let rs1_val = X(rs1);
    let rs2_val = X(0b0 @ imm[3 .. 0]);
    common_leakage(rs1_val, rs2_val);
    let t : xenbits = PC + EXTS(imm);
    let rd_next = get_next_pc();
    overwrite_leakage(rd, rd_next);
    X(rd) = get_next_pc();
    set_next_pc(t);
    RETIRE_SUCCESS
  } else RETIRE_FAIL
}

/* **************************** */
union clause ast =
RISC-V: (bits(13), regidx, regidx, bop)

mapping clause encdec_bop : bop <-> bits(3) = {
    RISCV_BEQ <-> 0b000,
    RISCV_BNE <-> 0b010,
    RISCV_BLT <-> 0b100,
    RISCV_BGE <-> 0b101,
    RISCV_BLTU <-> 0b110,
    RISCV_BGEU <-> 0b111
}

union clause encdec = BYTYPE(imm7_6 @ imm5_0 @ imm7_5_0 @
<= imm5_4_1 @ 0b0, rs2, rs1)
<= imm7_6 : bits(1) @ imm7_5_0 : bits(6) @ imm3 @ imm7_11, 11)
  function clause execute (BTYPE(imm, rs2, rs1, op)) = {
    let rs1_val = X(rs1);
    let rs2_val = X(rs2);
    common_leakage(rs1_val, rs2_val);
    let taken : bool = match op {
        RISCV_BEQ => rs1_val == rs2_val,
        RISCV_BNE => rs1_val != rs2_val,
        RISCV_BLT => rs1_val <_s rs2_val,
        RISCV_BGE => rs1_val >=_s rs2_val,
        RISCV_BLTU => rs1_val <_u rs2_val,
        RISCV_BGEU => rs1_val >=_u rs2_val
    };
    overwrite_leakage(0b00000, 0
    X(0b00000000000000000000000000000000);
    let t : xenbits = PC + EXTS(imm);
    if (t[1 .. 0] != 0b00) then
        return RETIRE_FAIL;
    if taken then { set_next_pc(t); }
    return RETIRE_SUCCESS
}

/* **************************** */
union clause ast =
RISCV_ADDI, RISCV_SLTI, RISCV_SLTIU, RISCV_XORI,
RISCV_ORI, RISCV_ANDI

mapping clause encdec_iop : iop <-> bits(3) = {
    RISCV_ADDI <-> 0b000,
    RISCV_SLTI <-> 0b010,
    RISCV_SLTIU <-> 0b011,
    RISCV_ANDI <-> 0b111,
    RISCV_ORI <-> 0b110,
    RISCV_XORI <-> 0b100
}

union clause ast =
ITYPE : (bits(12), regidx, regidx, iop)

mapping clause encdec_iop = ITYPE(imm, rs1, rd, op)
<= imm @ encdec_iop(op) @ rd @ 0b001
  function clause execute (ITYPE (imm, rs1, rd, op)) = {
    let rs1_val = X(rs1);
let rs2_val = X(0b0 @ imm[3 .. 0]);
common_leakage(rs1_val, rs2_val);
let immext = xlenbits = EXTS(imm);
let result : xlenbits = match op {
    RISCV_ADDI => rs1_val + immext,
    RISCV_SLTI =>
        EXTBOOL(rs1_val <_s immext),
    RISCV_SLTIU =>
        EXTBOOL(rs1_val <_u immext),
    RISCV_ANDI => rs1_val & immext,
    RISCV_ORI => rs1_val | immext,
    RISCV_XORI => rs1_val ^ immext,
    RISCV_SLTIU =>
        EXTBOOL(rs1_val ^ immext),
    RISCV_ADDI => rs1_val + immext,
    RISCV_ORI => rs1_val | immext,
    RISCV_XORI => rs1_val ^ immext
};
overwrite_leakage(rd, result);
X(rd) = result;
RETIRE_SUCCESS
}
/* **************************** */
enum sop = {RISCV_SLLI, RISCV_SRLI, RISCV_SRAI}
union clause ast =
    SHFIOP : (bits(6), regidx, regidx, sop)

mapping encdec_sop : sop <-> bits(3) = {
    RISCV_SLLI <-> 0b000000,
    RISCV_SRLI <-> 0b000000,
    RISCV_SRAI <-> 0b000000
}

mapping clause encdec = SHFIOP(shamt, rs1, rd, RISCV_SLLI)
<- 0b0000000 @ shamt @ rs1 @ 0b101 @ rd @ 0b0110011
    <- bitzero)

mapping clause encdec = SHFIOP(shamt, rs1, rd, RISCV_SRLI)
<- 0b0000000 @ shamt @ rs1 @ 0b000 @ rd @ 0b0010011
    <- bitzero)

mapping clause encdec = SHFIOP(shamt, rs1, rd, RISCV_SRAI)
<- 0b0010000 @ shamt @ rs1 @ 0b101 @ rd @ 0b0010011
    <- bitzero)

function clause execute (SHFIOP(shamt, rs1, rd, op)) = {
    let rs1_val = X(rs1);
    let rs2_val = X(0b0 @ shamt[3 .. 0]);
    common_leakage(rs1_val, rs2_val);
    /* the decoder guard ensures that shamt[5] = 0 for RV32E
    -> */
    let result : xlenbits = match op {
        RISCV_SLLI => if sizeof(xlen) == 32
            then shift_right_arith32(rs1_val, shamt
                
            )
        else shift_right_arith64(rs1_val, shamt);
        RISCV_SRLI => if sizeof(xlen) == 32
            then shift_right_arith32(rs1_val, shamt
                
            )
        else shift_right_arith64(rs1_val, shamt);
        RISCV_SRAI => if sizeof(xlen) == 32
            then shift_right_arith32(rs1_val, shamt
                
            )
        else shift_right_arith64(rs1_val, shamt);
        RISCV_SLTI =>
            EXTBOOL(rs1_val <_s immext),
        RISCV_SLTIU =>
            EXTBOOL(rs1_val <_u immext),
        RISCV_ANDI =>
            rs1_val & immext,
        RISCV_ORI =>
            rs1_val | immext,
        RISCV_XORI =>
            rs1_val ^ immext,
        RISCV_SLTIU =>
            EXTBOOL(rs1_val ^ immext),
        RISCV_ADDI =>
            rs1_val + immext,
        RISCV_ORI =>
            rs1_val | immext,
        RISCV_XORI =>
            rs1_val ^ immext
    }
    overwrite_leakage(rd, result);
    X(rd) = result;
    RETIRE_SUCCESS
}
function clause execute (RTYPE(rs2, rs1, rd, op)) = {
let rs1_val = X(rs1);
let rs2_val = X(rs2);
common_leakage(rs1_val, rs2_val);

let result : xlenbits = match op {
    RISCV_SRA => if sizeof(xlen) == 32
        then rs1_val >> (rs2_val[5..0]),
    else rs1_val >> (rs2_val[4..0]),
    RISCV_SUB => rs1_val - rs2_val,
    RISCV_SRL => if sizeof(xlen) == 32
        then shift_right_arith64(rs1_val, rs2_val[4..0])
    else shift_right_arith64(rs1_val, rs2_val[5..0]),
    RISCV_SLL => if sizeof(xlen) == 32
    RISCV_XOR => rs1_val ^ rs2_val,
    RISCV_OR => rs1_val | rs2_val,
    RISCV_AND => rs1_val & rs2_val,
    RISCV_SLTU => EXTZ(bool_to_bits(rs1_val <_u rs2_val)),
    RISCV_SLT => EXTZ(bool_to_bits(rs1_val <_s rs2_val)),
    RISCV_ADD => rs1_val + rs2_val,
    _ => unit effect {rreg, wreg, leakage}
}
}

function load_leakage(rs1_val : xlenbits, rs2_val : xlenbits)
    -> unit effect {rreg, wreg, leakage}
.

let req_addr = addr[(sizeof(xlen) - 1) .. 10];
let req_data = read_mem(Read_plain, sizeof(xlen), req_addr);
load Leakage(rs1_val, rs2_val, addr, req_data);
let req_byte : bits(8) = match (addr[1 .. 0]) {
    0b00 => req_data[ 7 .. 0],
    0b01 => req_data[15 .. 8],
    0b10 => req_data[23 .. 16],
    0b11 => req_data[31 .. 24];
    _ => RETIRE_FAIL // takes care of misaligned
};

/* **************************** */
enum word_width = {BYTE, HALF, WORD, DOUBLE}
union clause ast = LOAD :
    (bits(12), regidx, regidx, bool, word_width, bool, bool)

mapping clause encdec = LOAD(imm, rs1, rd, is_unsigned, size
    -> false, false)
if ((word_width_bytes(size) < sizeof(xlen_bytes))) |
    (not bool(is_unsigned) & word_width_bytes(size) <
    size(xlen_bytes))) & (rs1[4] == bitzero) & (rd
    -> [4] == bitzero)
<= imm @ rs1 @ bool_bits(is_unsigned) @ size_bits(size) @
    rd @ 0b0000011
if ((word_width_bytes(size) < sizeof(xlen_bytes))) |
    (not bool(is_unsigned) & word_width_bytes(size) <
    size(xlen_bytes))) & (rs1[4] == bitzero) & (rd
    -> [4] == bitzero)
function aligned(vaddr : xlenbits, width : word_width) ->
    bool =
    (width == BYTE | (width == HALF & vaddr[0] == bitzero) |
    (width == WORD & vaddr[1 .. 0] == 0b00))
val load Leakage : (xlenbits, xlenbits, xlenbits, xlenbits)
function clause execute (STORE(imm, rs2, rs1, width, aq, rl) => ) =
  let offset : xlenbits = EXTS(imm);
  let rs1_val = X(rs1);
  let rs2_val = X(rs2);
  common_leakage(rs1_val, rs2_val);
  let addr = rs1_val + offset;
  // address computation and register file access leakage
  leak(mem_last_addr, addr);
  // address computation and register file access leakage
  common_leakage(rs1_val, rs2_val);
  let rs2_val = X(rs2);
  let offset : xlenbits = EXTS(imm);
  let rs1_val = X(rs1);
  // overwrite_leakage(0b00000, result);
  let result = rs2_val + offset;
  // rewrite_mem(Write_plain, sizeof(xlen), addr, 4,
  // overflow_leakage(0b00000, result);
  let success : bool = match(width) {
    BYTE => write_mem(Write_plain, sizeof(xlen), addr, 1,
    HALF => write_mem(Write_plain, sizeof(xlen), addr, 2,
    WORD => write_mem(Write_plain, sizeof(xlen), addr, 4,
    _ => false);
  if success then {RETIRE_SUCCESS} else {RETIRE_FAIL}
} else { RETIRE_FAIL }

7.2 IBEX Configuration

In the following, we give the configuration file that specifies the mapping and normal operating conditions simultaneously.

Listing 7: IBEX configuration file

function clause execute (ILLEGAL(s)) =
  mapping clause encdec = ILLEGAL(s) <-> s
  return RETIRE_FAIL

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// SUCH DAMAGE.

// This file contains the configuration of our tool.
// It specifies
// - the state modeled in the contract (registers, memory,
//   leakage state)
// - the registers of the IBEX processor (registers and
//   memory)
// - a mapping between the states
// - which states may contain sensitive data
// - conditions which have to hold before/during execution
//   of an instruction
// - which HW and contract state is printed in
//   counterexamples

// Power Contract for IBEX
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contract register PC BitVec 32
hardware public u_ibex_core.pc_id
mapping register PC u_ibex_core.pc_id

next PC
hardware public u_ibex_core.if_stage_i.gen_prefetch_buffer.
  prefetch_buffer_i.fifo_i.instr_addr_q
contract register nextPC BitVec 32
mapping register nextPC u_ibex_core.if_stage_i.
  gen_prefetch_buffer.prefetch_buffer_i.fifo_i.
  instr_addr_q

contract REGISTERS

contract register x1 BitVec 32
contract register x2 BitVec 32
contract register x3 BitVec 32
contract register x4 BitVec 32
contract register x5 BitVec 32
contract register x6 BitVec 32
contract register x7 BitVec 32
contract register x8 BitVec 32
contract register x9 BitVec 32
contract register x10 BitVec 32
contract register x11 BitVec 32
contract register x12 BitVec 32
contract register x13 BitVec 32
contract register x14 BitVec 32
contract register x15 BitVec 32

memory raddr u_ibex_core.load_store_unit.i.adder_result_ex_i ↦ read_addr_1
memory rdata data_rdata_i read_val_1
memory req data_req_o
memory gnt data_gnt_i
memory ack data_val_i
memory data data_we_o

hardware const@pre u_ibex_core.instr_id_done 0b1
hardware const@start u_ibex_core.id_stage_i.decoder_i. illegal_insn 0b0

hardware const@pre: rst_ni 0b1
hardware const@end-1 u_ibex_core.id_stage.i.decoder_i. illegal_insn 0b0

hardware const@pre u_ibex_core.if_stage.i.fetch_valid 0b1
hardware const@end-1 u_ibex_core.if_stage.i.fetch_valid 0b1

memory raddr u_ibex_core.load_store_unit.i.adder_result_ex_i ↦ read_addr_1
memory rdata data_rdata_i read_val_1
memory req data_req_o
memory gnt data_gnt_i
memory ack data_val_i
memory data data_we_o

contract opcode op BitVec 32

memory raddr u_ibex_core.load_store_unit.i.adder_result_ex_i ↦ read_addr_1
memory rdata data_rdata_i read_val_1
memory req data_req_o
memory gnt data_gnt_i
memory ack data_val_i
memory data data_we_o

contract opcode op BitVec 32

memory raddr u_ibex_core.load_store_unit.i.adder_result_ex_i ↦ read_addr_1
memory rdata data_rdata_i read_val_1
memory req data_req_o
memory gnt data_gnt_i
memory ack data_val_i
memory data data_we_o
法律规定

hardware public clk_i
hardware public ram_cfg_i
hardware public test_en_i
hardware public hart_id_i
hardware public boot_addr_i
// Instruction memory interface
hardware public instr_gnt_i
hardware public instr_rvalid_i
hardware public data_gnt_i
hardware public data_rvalid_i
hardware public data_err_i
hardware const@pre: data_err_i 0b0
// interrupts
hardware public irq_software_i
hardware public irq_timer_i
hardware public irq_external_i
hardware public irq_fast_i
hardware public irq_mm_i
// disabling interrupts
hardware const@pre: irq_software_i 0b0
hardware const@pre: irq_timer_i 0b0
hardware const@pre: irq_external_i 0b0
hardware const@pre: irq_fast_i 0b0000000000000000
hardware const@pre: irq_mm_i 0b0
// core debug
hardware public debug_req_i
hardware const@pre: debug_req_i 0b0
hardware public fetch_enable_i
hardware public scan_rst_ni
 hardware public u_ibex_core.load_store_unit_i.instr_last_addr

// instruction decode
hardware public u_ibex_core.id_stage_i.controller_i.
\(\leftarrow\) ctrl_fsm_cs
hardware public u_ibex_core.id_stage_i.controller_i.
\(\leftarrow\) load_err_q
hardware public u_ibex_core.id_stage_i.controller_i.
\(\leftarrow\) store_err_q
hardware public u_ibex_core.id_stage_i.controller_i.
\(\leftarrow\) exc_req_q
hardware public u_ibex_core.id_stage_i.branch_set_raw
hardware const@start u_ibex_core.id_stage_i.branch_set_raw \(\leftarrow\) b0
// since data_err_i is never 1 and pmp_err_q is also not 1,
// this must be 0
hardware public u_ibex_core.load_store_unit_i.lsu_err_q
hardware const@start u_ibex_core.load_store_unit_i.lsu_err_q
\(\leftarrow\) 0b0
hardware public u_ibex_core.load_store_unit_i.data_we_q
hardware public u_ibex_core.load_store_unit_i.data_we_q
\(\leftarrow\) handle_disaligned_q
hardware public u_ibex_core.id_stage_i.controller_i.
\(\leftarrow\) illegal_insn_q
hardware public u_ibex_core.id_stage_i.controller_i.
\(\leftarrow\) do_single_step_q
hardware public u_ibex_core.id_stage_i.controller_i.
\(\leftarrow\) enter_debug_mode_prio_q
// LSU register handling misaligned memory accesses which
// are not allowed by the contract
hardware public u_ibex_core.load_store_unit_i.rdata_q
contract leakagestate mem_last_read BitVec 32
// must be idle when new instruction reaches ID/EX
hardware public u_ibex_core.load_store_unit_i.ls_fsm_cs
hardware const@start u_ibex_core.load_store_unit_i.ls_fsm_cs
\(\leftarrow\) 0b0000
hardware variable u_ibex_core.load_store_unit_i.addr_last_q
hardware variable u_ibex_core.load_store_unit_i.
\(\leftarrow\) rdata_offset_q
contract leakagestate mem_last_addr BitVec 32
mapping leakagestate mem_last_addr u_ibex_core.
  \rightarrow load_store_unit_i.addr_last_q

mapping leakagestate mem_last_addr u_ibex_core.
  \rightarrow load_store_unit_i.rdata_offset_q

hardware public u_ibex_core.load_store_unit_i.data_type_q
  \rightarrow data_sign_ext_q

// system registers

hardware public u_ibex_core.cs_registers_i.mie_q
hardware public u_ibex_core.cs_registers_i.mtval_q
hardware public u_ibex_core.cs_registers_i.mcause_q
hardware public u_ibex_core.cs_registers_i.mscratch_q
hardware public u_ibex_core.cs_registers_i.mscratch0_q
hardware public u_ibex_core.cs_registers_i.mscratch1_q
hardware public u_ibex_core.cs_registers_i.mstatus_q
hardware public u_ibex_core.cs_registers_i.mcountinhibit
hardware public u_ibex_core.cs_registers_i.mhpmcounter[0]
hardware public u_ibex_core.cs_registers_i.mhpmcounter[1]
hardware public u_ibex_core.cs_registers_i.mhpmcounter[2]

// hardware constants

hardware const@start u_ibex_core.cs_registers_i.dcsr_q 0
  \rightarrow b00000000000000000000000000000000

hardware public u_ibex_core.cs_registers_i.mhpmcounter[0]
hardware public u_ibex_core.cs_registers_i.mhpmcounter[1]
hardware public u_ibex_core.cs_registers_i.mhpmcounter[2]

contract leakagestate rf_pA BitVec 32
contract leakagestate rf_pB BitVec 32