Towards Practical PFE: An Efficient 2-Party Private Function Evaluation Protocol Based on Half Gates

Osman Biçer[1], Muhammed Ali Bingöl[2,3], Mehmet Sabır Kiraz[3],, and Albert levi[2]

[1] İstanbul Şehir University
osmnbicr@gmail.com
[2] Sabancı University
levi@sabanciuniv.edu
[3] TÜBİTAK BİLGEM
{muhammedali.bingol, mehmet.kiraz}@tubitak.gov.tr

Abstract. Private function evaluation (PFE) is a special case of secure multi-party computation (MPC), where the function to be computed is known by only one party. PFE is useful in several real-life settings where an algorithm or a function itself needs to remain secret due to its confidential classification or intellectual property. In this work, we look back at the seminal PFE framework presented by Mohassel and Sadeghian at Eurocrypt'13. We show how to adapt and utilize the well-known *half gates* garbling technique (Zahur *et al.*, Eurocrypt'15) to their constant round 2-party PFE scheme. Compared to their scheme, our resulting optimization considerably improves the efficiency of both the underlying *Oblivious Evaluation of Extended Permutation* (OEP) and secure 2-party computation (2PC) protocol, and yields a more than 40% reduction in overall communication cost (the computation time is also slightly decreased, and the number of rounds remains unchanged).

1 Introduction

Suppose that one invents a novel and practical algorithm capable of being directly used to detect and identify criminals in crowds with a high degree of precision based on information about their behaviors obtained from street video recordings. It is obvious that this algorithm would be precious and that many governmental organizations would pay millions to apply it. The inventor of the algorithm has the right to keep the algorithm commercially confidential, and to offer only its use for a certain fee since it is her own intellectual property. On the other hand, governmental organizations will generally be unwilling to reveal their databases and records to the parties to whom they do not sufficiently trust. This and such problems have been addressed by *private function evaluation* (PFE).

PFE is a special case of secure multi-party computation (MPC) in which n participants jointly compute a function f on their private inputs $x_1, \ldots, x_n$, and obtain the result $f(x_1, \ldots, x_n)$. The difference of PFE from the standard MPC setting is that here the function f is also a private input of one of the participants[4]. A PFE solution would be more useful than conventional MPC in various applications, *e.g.*, the ones where the function itself contains private information, or reveals security weaknesses; or the ones where service providers prefer hiding their function or its specific implementation as their intellectual property. The task of designing efficient PFE protocols for special or generic purposes is addressed in several papers in literature [1–6].

Generic PFE solutions are mainly classified into two categories. The first one is the *universal circuit* [7] based approach that works with any MPC protocol. The ideal functionality of MPC $\mathcal{F}_{U_g}$ for a universal circuit U_g takes as input a certain sized (g) boolean circuit representation $\mathcal{C}_f$ of the private function f, and inputs of parties $x_1, \ldots, x_n$ (*i.e.*, $\mathcal{F}_{U_g}(\mathcal{C}_f, x_1, \ldots, x_n)$), and outputs $f(x_1, \ldots, x_n)$. The works based on this approach mainly aim to reduce the size of

[4] Note that PFE also covers the case where the party who knows the function does not have any other private input.

universal circuits, and to optimize their implementations using some MPC techniques [1, 2, 8, 9]. Unfortunately, existing universal circuit based schemes result in massive circuit sizes, which is the root cause of their inefficiency. Therefore, some recent PFE solutions avoid using universal circuits for the sake of practicality [4–6]. An early attempt on this second category is Paus, Sadeghi, and Schneider's work [4]. They introduce -what they called- a *semi-private function evaluation* in which the type of the gates is a secret of one party, but the circuit topology (*i.e.*, the set of all connections of predecessors and successors of each gate) is public to both parties. Due to the weaker assumption of semi-privacy, their approach does not provide a complete PFE solution. Another significant improvement in this category comes from Katz and Malka's 2-party PFE (2-PFE) scheme with a mechanism for hiding the circuit topology based on singly homomorphic encryption [5]. Although their scheme is favorable in terms of asymptotic complexity, its high computational cost unfortunately makes its use impractical.

In [6], Mohassel and Sadeghian come up with a prominent and efficient PFE framework which ensures hiding the topology of the circuit. It has been basically designed for the semi-honest model, and later generalized to the malicious case by Mohassel, Sadeghian and Smart [10]. Their generic PFE framework can be applied to both arithmetic and boolean circuits. Considering the 2-party boolean circuit based scheme, they split the PFE task into two sub-functionalities: (1) Circuit topology hiding (CTH), (2) Private gate evaluation (PGE). Briefly speaking, in CTH, a series of procedures is performed: First, the function owner (say P_1) detaches the interconnections of the gates to obtain single gates, and keeps the topological mapping of the circuit private. Second, P_1 and the other party (say P_2) engage in an *oblivious evaluation of switching network* (OSN)[5] protocol which consists of $O(g\mathsf{lg}(g))$ *oblivious transfer* (OT) operations (throughout this paper, g denotes the number of gates, and $\mathsf{lg}()$ denotes the logarithm base 2). Next, in PGE, both parties engage in a Yao's 2-party computation (2PC) protocol [11, 12] where P_1 and P_2 play the *evaluator* and the *garbler* roles, respectively. Each single gate is garbled into four ciphertexts. By setting all gates as a single gate type (*e.g.*, NAND or NOR), it is possible to avoid the necessity of hiding the gate functionality [6].

Recently, in [13], Wang and Malluhi attempt to improve the 2-PFE scheme of Mohassel and Sadeghian by removing only one ciphertext from each garbled gate in the 2PC phase. However, the communication cost of the 2PC phase is quite lower than that of the OSN phase, which means that their scheme reduces the overall cost by less than 1% (see Table 7).

Our contributions. One of the primary objectives of the recent research on MPC, and specifically PFE, is minimizing the communication cost. This is due to the fact that historical developments in hardware technology show us computing power advances faster than communication channels. This is even more likely to be so in the near future, *i.e.*, the constriction for many secure computation applications will not be the CPU load but be the bandwidth constraints [14, 15]. Motivated by this, we are mainly interested in reducing the communication complexity of the 2-PFE protocol. In this respect, we first revisit the Mohassel and Sadeghian's pioneering PFE framework [6], then propose a more efficient protocol (secure in the presence of semi-honest adversaries) by adapting [6] the state-of-the-art half gates garbling optimization [16] to their 2-PFE scheme. Our protocol achieves the following improvements in both OSN and 2PC phases:

[5] The OSN mechanism is introduced in [6] to achieve a solution for the oblivious evaluation of extended permutation (OEP) problem. OEP allows the oblivious transition of each masked gate output to the input(s) of the next connected gate(s).

[6] Note that in [13], Wang and Malluhi mention that free-XOR and half gates techniques cannot be used to improve the efficiency of non-universal circuit based PFE protocols such as Katz and Malka's [5] and Mohassel and Sadeghian's [6] works. In contrast to their claim, we adapt and utilize half gates approach to [6] to reduce the communication cost.

1. Regarding the OSN phase: (1) We reduce the number of required OTs by $N = 2g$. Concretely, [6] requires $2N\lg N+1$ OTs, while our protocol requires $2N\lg N - N + 1$ OTs. Besides the bandwidth savings, this improvement yields a slight reduction in the computation cost. (2) Our protocol reduces the data sizes entering to the OSN protocol by a factor of 2. This improvement results in about 40% saving in the transferred number of bits.
2. Regarding the 2PC phase, our scheme garbles each non-output gate (that does not have any direct connection with output wires) with only three ciphertexts, and each output gate with only two ciphertexts. This improvement further reduces the communication cost.

No. of	**Overall Communication Cost**		**Overall**
Gates	**MS'13** [6]	**Our Scheme**	**Reduction**
2^8	752KB	436KB	42.0%
2^{10}	3.56MB	2.08MB	41.7%
2^{12}	16.8MB	9.8MB	41.4%
2^{14}	77.0MB	45.3MB	41.2%
2^{16}	348MB	205MB	41.1%
2^{18}	1.52GB	0.89GB	41.0%
2^{20}	6.69GB	3.95GB	40.9%

Table 1. Comparison of two schemes with respect to overall communication cost. The security parameter (λ) is assumed to be 128.

Among the above improvements, the foremost gain comes from the reduction in the input sizes of the OSN protocol. The overall communication cost of our scheme is $(6N\lg N + 0.5N + 3)\lambda$ bits[7], which is a significant improvement compared to [6], whose communication cost is $(10N\lg N+4N+5)\lambda$ bits. This means more than 40% saving in bandwidth size. Table 1 illustrates the comparison of two schemes in terms of communication cost for various circuit sizes (see also Table 7 for a more detailed comparison).

Organization. In Section 2, we give preliminary information about oblivious transfer, Yao's garbled circuits, and half gates optimization. In Section 3, we present the 2-PFE framework and scheme of [6] in detail. In Section 4, we introduce our 2-party PFE protocol and analyze its security in the semi-honest model. In Section 5, we analyze our protocol in terms of communication and computation complexities and compare it with 2-PFE scheme in [6]. Finally, Section 6 concludes the paper with projecting forward to future work.

2 Preliminaries

This section provides some background information on oblivious transfer, Yao's garbled circuits, and the state-of-the-art half gates optimization.

2.1 Oblivious transfer

A *k-out-of-m oblivious transfer* protocol is a two-party protocol where one of the parties is the sender ($\mathcal{S}$) who has set of values $\{x_1, \ldots, x_m\}$, and the other one is the receiver ($\mathcal{R}$) who has

[7] λ is the security parameter throughout this paper.

k selection indices. At the end of the protocol, $\mathcal{R}$ only learns k of the $\mathcal{S}$'s inputs according to his selection indices; whereas $\mathcal{S}$ learns nothing. Oblivious transfer (OT) is a critical underlying protocol used in many MPC constructions [17, 18].

OT extension is a way of obtaining many OTs from a few number of OT runs and cheap symmetric cryptographic operations. Ishai *et al.* constructed the first OT extension method [19], which reduces a given large number of required OTs to a fixed size security parameter. Later, several OT extension schemes based on [19] are proposed for improving the efficiency [20, 21].

2.2 Yao's protocol

Yao's protocol is essentially a 2PC protocol secure in the semi-honest adversary model. It allows two parties, the *garbler* and the *evaluator*, to evaluate an arbitrary polynomial-sized function $f(x) = f(x_1, x_2)$, where x_1 is the garbler's private input and x_2 is the evaluator's private input, without leaking any information about their private inputs to each other beyond what is implied by the pure knowledge of the function output. The main idea is that the garbler prepares an *encrypted* version of $\mathcal{C}_f$ (a boolean circuit representation of f). This encrypted version is called the garbled circuit $\hat{F}$ and sent to the evaluator. The evaluator then computes the output from the garbled version of the circuit without obtaining the garbler's input bits or intermediate values.

Recently, several major optimizations proposed for Yao's protocol, mainly aiming at bandwidth efficiency and or reduction of the garbling and evaluating costs (*e.g.*, garbled row reduction 3 ciphertexts (GRR3) [22], free-XOR [23], garbled row reduction 2 ciphertexts [15], pipelining [24], fleXOR [14], half gates [16] and [25]). With the recent optimizations, Yao's protocol has now impressive results from the complexity point of view.

Garbler half gate (p_b known to the garbler)	**Evaluator half gate ($p_b \oplus v_b$ known to the evaluator)**
Defines the half gate:	Defines the half gate:
$f_G(v_a, p_b) := (\alpha_1 \oplus v_a)(\alpha_2 \oplus p_b) \oplus \alpha_3$	$f_E(v_a, v_b \oplus p_b) := (\alpha_1 \oplus v_a)(p_b \oplus v_b)$
Computes:	Computes:
$T_{Gc} \leftarrow H(w_a^0) \oplus H(w_a^1) \oplus (p_b \oplus \alpha_2)R$	$T_{Ec} \leftarrow H(w_b^0) \oplus H(w_b^1) \oplus w_a^{\alpha_1}$
$w_{Gc}^0 \leftarrow H(w_a^{p_a}) \oplus f_G(p_a, p_b)R$	$w_{Ec}^0 \leftarrow H(w_b^{p_b})$
The garbler sends T_{Gc}.	The garbler sends T_{Ec}.

Table 2. Garbling an odd gate using half gates technique [16].

2.3 Half gates technique

In [16], Zahur, Rosulek, and Evans propose an elegant and efficient garbling scheme called *half gates*. Their garbling technique is currently known the most efficient optimization in terms of communication complexity compared to any prior scheme. This technique remains compatible with free-XOR [23] while also reducing the ciphertext requirement for each odd gate[8] to two.

[8] *Odd* and *Even* gates are fan-in-2 gates. The former has an odd number of TRUE outputs in its truth table; while the latter has an even number of those.

Here, we briefly describe the garbling procedure of odd gates using the half gates technique, and refer the reader to [16] for further details and its security proof.

Any odd gate type can be written as Equation (2.1) where α_1, α_2 and α_3 define the gate type, *e.g.*, setting $\alpha_1 = 0$, $\alpha_2 = 0$, $\alpha_3 = 1$ results in a NAND gate [16]. Let v_i denote the one bit truth value on the i^{th} wire in a circuit.

$$f_{G_{\text{odd}}}(v_a, v_b) \to (\alpha_1 \oplus v_a) \wedge (\alpha_2 \oplus v_b) \oplus \alpha_3 \tag{2.1}$$

The garbler garbles an odd gate by following the steps for both half gates in Table 2. The tokens for FALSE and TRUE on the i^{th} wire are denoted as w_i^0 and w_i, respectively. The global free-XOR offset is denoted as R. The garbler sets $R \twoheadleftarrow \{0,1\}^{\lambda-1}1$ globally, and $w_i^0 \twoheadleftarrow \{0,1\}^\lambda$ and $w_i^1 \leftarrow w_i^0 \oplus R$ for each wire. We have $\mathsf{lsb}(R) = 1$ so that $\mathsf{lsb}(w_i^0) \neq \mathsf{lsb}(w_i^1)$. w_{Gc}^{b} and w_{Ec}^{b} denote the tokens for the garbler and the evaluator half gate outputs for truth value b, respectively. T_{Gc} and T_{Ec} denote the λ-bit strings needing to be sent for the garbler and evaluator half gates, respectively. Let w_i be a token on i^{th} wire obtained by the evaluator who does not know its corresponding truth value v_i. For the ith wire, let $p_i := \mathsf{lsb}(w_i^0)$, a value only known to the garbler. If two symbols are appended, an AND operation is implied, *i.e.*, $ab = a \wedge b$. $H : \{0,1\}^\lambda \times \mathbb{Z} \to \{0,1\}^\lambda$ denotes a hash function with circular correlation robustness for naturally derived keys[9], having the security parameter λ.

The token on the output wire of the odd gate for FALSE is $w_{Gc}^0 \oplus w_{Ec}^0$ since the output of the odd gate is an XOR of half gate outputs. The two ciphertexts computed T_{Gc} and T_{Ec} is needed to be sent to the evaluator for each gate.

3 2-Party PFE Framework

In [6], Mohassel and Sadeghian present a generic PFE framework for boolean and arithmetic circuits in multi-party case. However, in this work, our focus is mainly on boolean circuits in 2-party setting. Throughout this paper the party who knows the private function is called P_1, also playing the evaluator role in 2PC; whereas the other party is be called P_2, also playing the garbler role in 2PC. In order to achieve 2-PFE, Mohassel and Sadeghian show that hiding the parties' private inputs, the topology of the boolean circuit representation $\mathcal{C}_f$ of private function, and the functionality of its gates is required. The framework is not concerned with hiding the numbers of gates, input/output wires, and the type of the gates of the circuit. The complete task of PFE is classified into two functionalities: (1) Circuit Topology Hiding (CTH), (2) Private Gate Evaluation (PGE).

In a nutshell, in CTH, P_1 extracts the topological mapping π_f (kept private) from the circuit representation $\mathcal{C}_f$, and converts the whole circuit into a collection of single gates. Then P_1 and P_2 engage in an *oblivious evaluation of switching network* (OSN) protocol where P_2 obliviously obtains tokens on gate inputs. In PGE, a 2PC protocol is performed to obtain the final output.

In the rest of this section, we describe the notions related to CTH, and the 2-PFE scheme proposed in [6].

3.1 Context of CTH

Let g, n and m denote the number of gates (size), the number of inputs and the number of outputs of $\mathcal{C}_f$, respectively. OW denotes the set of outgoing wires which is the union of the input wires of the circuit and the output wires of its non-output gates (having $M = n+g-m$ elements

[9] *Circular correlation robustness for naturally derived keys* is the security requirement for a suitable hash function used in half gates garbling. We refer the reader to [16] for its details.

in total *whose indices are chosen randomly*): $\{\mathsf{ow}_1, \ldots, \mathsf{ow}_{n+g-m}\}$. Similarly, IW denotes the set of incoming wires which is the input wires of each gate in the circuit (having $N = 2g$ elements in total *whose indices are chosen randomly*): $\{\mathsf{iw}_1, \ldots, \mathsf{iw}_{2g}\}$.

The full description of the topology of a boolean circuit $\mathcal{C}_f$ can be accomplished by a mapping $\pi_f : \mathsf{OW} \rightarrow \mathsf{IW}$. The mapping π_f maps i to j (*i.e.*, $\pi_f(i) \rightarrow j$), if and only if $\mathsf{ow}_i \in \mathsf{OW}$ and $\mathsf{iw}_j \in \mathsf{IW}$ correspond to the same wire in the circuit $\mathcal{C}_f$. Note that the mapping π_f is not a function if an outgoing wire corresponds to more than one incoming wire, while its inverse π_f^{-1} is always a function. Figure 1 shows an example circuit $\mathcal{C}_f$ and its mapping π_f.

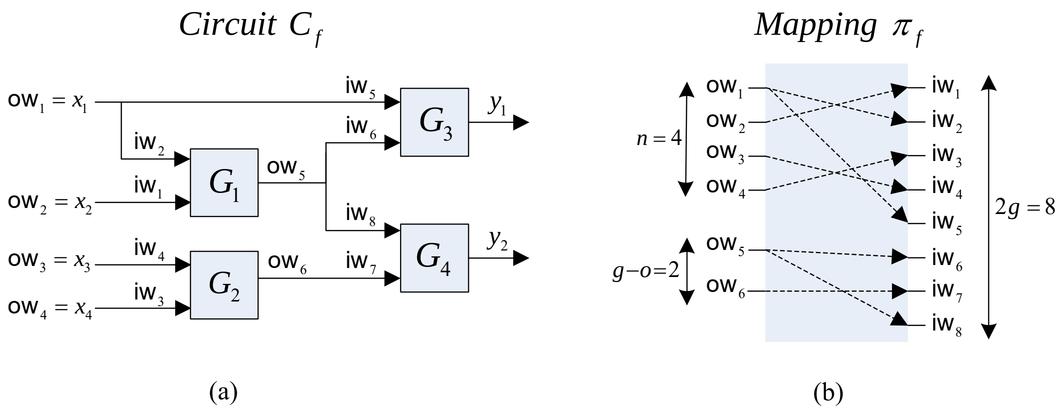


Fig. 1. (a) A circuit representation $\mathcal{C}_f$ of a function f. (b) The mapping π_f of f.

From the inclusion-exclusion principle, we obtain Equation (3.2) that gives the number of possible mappings for the given M and N values.

$$\rho = \sum_{i=0}^{M} (-1)^i \binom{M}{i} (M-i)^N \tag{3.2}$$

In the context of CTH, ρ indicates the number of possible circuit topologies. Thus, the security of CTH is proportional to ρ.

In what follows, we describe the main elements of CTH functionality whose essential target is the oblivious application of the mapping π_f.

Oblivious evaluation of mapping. A mapping $\pi : \{1, \ldots, N\} \rightarrow \{1, \ldots, N\}$ is a permutation if it is a bijection. We next define the *extended permutation* (EP) as follows:

Definition 1 (Extended permutation (EP)). *Given the positive integers M and N, a mapping $\pi : \{1, \ldots, M\} \rightarrow \{1, \ldots, N\}$ is called an EP if for all $y \in \{1, \ldots, N\}$, there exists a unique $x \in \{1, \ldots, M\}$ such that $\pi(x) = y$.*

The 2-party oblivious evaluation of extended permutation (2-OEP) functionality is defined as follows:

Definition 2 (2-OEP functionality). *The first party P_1's inputs are an EP $\pi : \{1, \ldots, M\} \rightarrow \{1, \ldots, N\}$, and a blinding vector for incoming wires $T := [t_j \twoheadleftarrow \{0,1\}^\lambda]$ for $j = 1, \ldots, N$. The other party P_2's inputs are a vector for outgoing wires $W := [w_i \twoheadleftarrow \{0,1\}^\lambda]$ for $i = 1, \ldots, M$. At the end, P_2 learns $S := [\sigma_j = w_{\pi_f^{-1}(j)} \oplus t_j]$ for $j = 1, \ldots, N$ while P_1 learns nothing.*

We call any 2-party protocol construction realizing the 2-OEP functionality as a *2-OEP protocol*. Mohassel and Sadeghian have constructed a constant round 2-OEP protocol by introducing the OSN structure. Since we also utilize their 2-OEP protocol in our scheme, here we give some of its details. Mainly, they first construct an extended permutation using switching networks, then provide a method using OTs for oblivious evaluation of the resulting switching network. We refer our reader to [6] for the security proof and application of this construction on various MPC protocols.

EP construction from switching networks. Each 2-switch takes two λ-bit strings and two selection bits as input, outputting two λ-bit strings [6]. Each of the outputs may get the value of any of the input strings depending on the selection bits. This means for input values (x_0, x_1), there are four different switch output possibilities. The two selection bits s_0 and s_1 are used for determining the switch output (y_0, y_1). In particular, the switch outputs $y_0 = x_{s_0}$, and $y_1 = x_{s_1}$.

Unlike 2-switches, 1-switches have only one selection bit s. For an input (x_0, x_1), a 1-switch outputs one of the two possible outputs: (x_0, x_1) if $s = 0$, and (x_1, x_0) otherwise.

Definition 3 (Switching Network (SN)). *A switching network SN is a collection of interconnected switches whose inputs are N λ-bit strings and a set of selection bits of all switches, and whose outputs are N λ-bit strings.*

The mapping $\pi : \{1, \ldots, N\} \to \{1, \ldots, N\}$ related to an SN ($\pi(i) = j$) implies that when the SN is executed, the string on the output wire j gets the value of that on the input wire i.

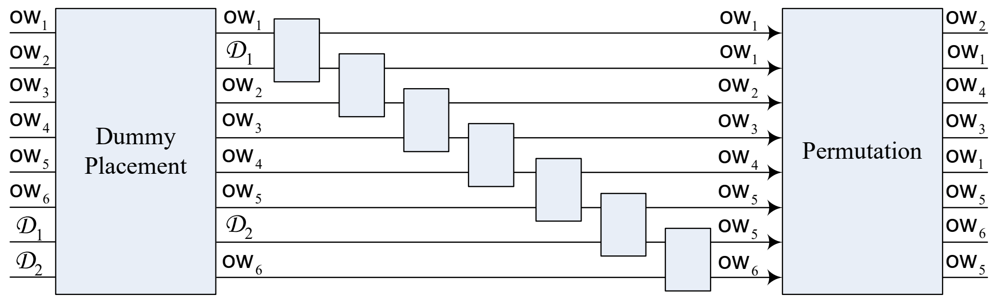


Fig. 2. The related switching network for the mapping π_f in Figure 1.

A *permutation network* PN is a special SN whose mapping is a permutation of its inputs. In contrast to SNs, PNs compose of 1-switches.

Waksman proposes an efficient PN construction in [26]. Mainly, this work suggests that a PN with $N = 2^\kappa$ inputs can be constructed with $N \lg N - N + 1$ switches.

In [6], the authors propose the construction of an extended permutation by combining SNs and PNs. However, extended permutations differ from SNs in that the number of their inputs M and that of their outputs N need not be equal ($M \leq N$). $N - M$ additional dummy inputs are added to the real inputs of an EP $\pi : \{1, \ldots, M\} \to \{1, \ldots, N\}$ in order to simulate it as an SN.

The SN design for extended permutation is divided into three components (see also Figure 2):

1. **Dummy placement component.** Dummy placement component takes N input strings composing of real and dummy ones. For each real input that π maps to k different outputs, the dummy-value placement component's output is the real string followed by $k - 1$ dummy strings.

2. **Replication component.** Replication component takes the output of the dummy-value placement component as input. If a value is real, it goes unchanged. If it is a dummy value, it is replaced by the real value which precedes it. This can be computed by a series of $N-1$ 2-switches whose selection bits (s_0, s_1) are either (0,0) or (0,1). If the selection bits are (0,0), that means x_1 is dummy, and x_0 goes both of the outputs. If they are (0,1), that means both inputs are real, and both are kept on the outputs in the same order. At the end of this step, all the dummy inputs are replaced by the necessary copies of the real inputs.
3. **Permutation component.** Permutation component takes the output wires of the replication component as input. It outputs a permutation of them so that each string is placed on its final location according to the prescription of mapping π.

An efficient implementation of both dummy placement and permutation blocks is via the use of a Waksman permutation network. Combining the three components, one gets a larger switching network, where the number of switches needed is $2(N\mathsf{lg}N - N + 1) + N - 1 = 2N\mathsf{lg}N - N + 1$ [6]. The topology of the whole switching network is the same for all N input EPs, and the selection bits specify the input values appearing on the outputs.

Oblivious evaluation of SN construction (OSN). We continue with describing Mohassel and Sadeghian's method for oblivious evaluation of switching networks using OTs.

Adapting the switching network construction to the 2-OEP functionality, P_1 produces the selection bits of the switching network using π, and has a blinding vector T. P_2 has an input vector for outgoing wires W. At the end, P_2 learns the switching network's blinded output vector for incoming wires S, and P_1 learns $\perp$. We describe the oblivious evaluation of one of its building block, *i.e.*, a single 2-switch u.

Let the input wires of the 2-switch be a and b, and its output wires be c and d. Each of the four wires of the switch has a uniformly random string assigned by P_2 as her share of that wire in the preparation stage, namely, $r_a, r_b, r_c, r_d \twoheadleftarrow \{0,1\}^\lambda$ for a, b, c, d, respectively. P_1 has the strings $w_1 \oplus r_a$ and $w_2 \oplus r_b$ as his shares for the two input wires. The purpose is enabling P_1 to obtain his output shares according to his selection bits. There are four possibilities for P_1's output shares depending on his selection bits s_{0u} and s_{1u} (see Table 3).

(s_{0u}, s_{1u})	y_0	y_1
(0,0)	$w_1 \oplus r_c$	$w_1 \oplus r_d$
(0,1)	$w_1 \oplus r_c$	$w_2 \oplus r_d$
(1,0)	$w_2 \oplus r_c$	$w_1 \oplus r_d$
(1,1)	$w_2 \oplus r_c$	$w_2 \oplus r_d$

Table 3. P_1 learns one of these rows according to his selection bits.

P_2 prepares a table with four rows using r_a, r_b, r_c, r_d (see Table 4). P_1 and P_2 engage in a 1-out-of-4 OT in which P_2 inputs the four rows that she has prepared, and P_1 inputs his selection bits for the switch u. At the end, P_1 learns one of the rows as the output in the table. Assume that P_1's selection bits are (1,0). This means P_1 retrieves the third row, *i.e.*, $(r_b \oplus r_c, r_a \oplus r_d)$. According to the his selection bits, P_1 XORs his input share $w_2 \oplus r_b$ with $r_b \oplus r_c$, as well as his other input share $w_1 \oplus r_a$ with $r_a \oplus r_d$, and obtains his output shares $w_2 \oplus r_c$ and $w_1 \oplus r_d$.

The oblivious evaluation of the entire SN for EP goes as follows. In an offline stage, P_2 sets a uniformly random λ-bit string to each wire in the switching network. P_2 blinds each

(s_{0u},s_{1u})	Ω_0	Ω_1
(0,0)	$r_a \oplus r_c$	$r_a \oplus r_d$
(0,1)	$r_a \oplus r_c$	$r_b \oplus r_d$
(1,0)	$r_b \oplus r_c$	$r_a \oplus r_d$
(1,1)	$r_b \oplus r_c$	$r_b \oplus r_d$

Table 4. P_1 gets one of these rows by engaging in 1-out-of-4 OT with P_2.

element of her input vector W and the dummy strings which she assigned for $N - M$ inputs of the switching network with her corresponding shares for input wires (an XOR operation is involved in each blinding). P_2 prepares tables for each switch in the switching network similar to Table 3 and Table 4. However, both tables for each switch in this scenario has two rows since each switch, in fact, has two possible outputs[10]. This means each switch in the entire switching network can be evaluated running 1-out-of-2 OT. Moreover, the construction permits parallel OT runs and or use of OT extension, resulting in a constant round scheme. P_2 needs to send her blinded inputs to P_1, which can be done during her turn in OT extension in order not to increase the round complexity unnecessarily. Once P_1 gets P_2's blinded inputs which are also his input shares and the outputs of all OTs, he evaluates the entire switching network in topological order, obtaining his output shares. P_1 blinds his output shares with corresponding elements of T (again, an XOR operation is involved in each blinding), and sends the resulting vector to P_2. P_2 unblinds each element using her shares for output wires, and obtains the OEP output S. The extended permutation in this construction includes $2N\mathsf{lg}N - N + 1$ switches in total, requiring $2N\mathsf{lg}N - N + 1$ OTs for their oblivious evaluation.

3.2 Mohassel and Sadeghian's 2-PFE scheme

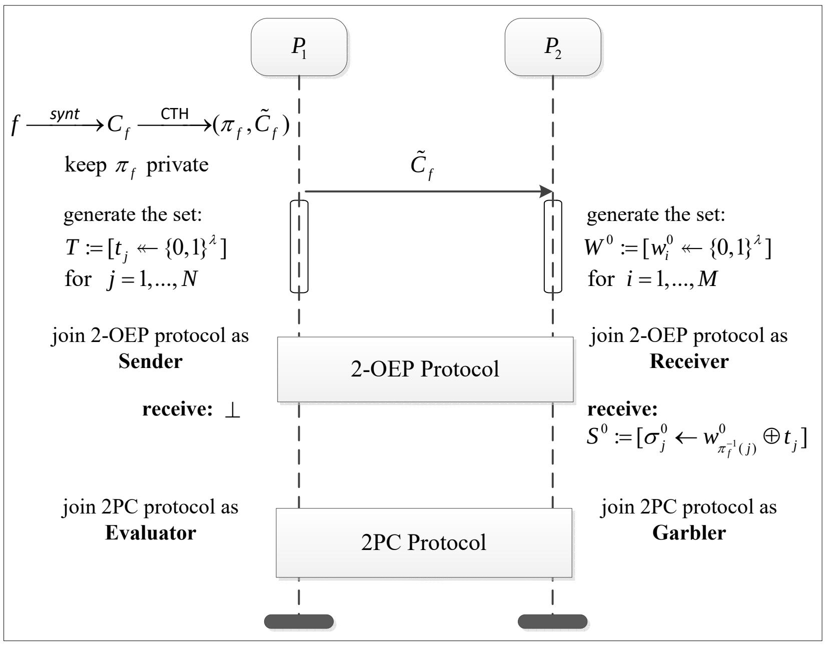
Here we provide an outline of Mohassel and Sadeghian's 2-PFE construction, and refer the reader to their work for detailed information and its security proof [6]. Their protocol is as follows. P_2 first randomly generates tokens $w_i^0, w_i^1 \twoheadleftarrow \{0,1\}^\lambda$ for each $\mathsf{ow}_i \in \mathsf{OW}$ corresponding to FALSE and TRUE, respectively. P_1 also generates random blinding strings $t_j^0, t_j^1 \twoheadleftarrow \{0,1\}^\lambda$ for each $\mathsf{iw}_j \in \mathsf{IW}$. And then P_1 and P_2 engage in OSN slightly modified from their 2-OEP protocol, where at the end, P_2 learns $[\sigma_j^0 = w^0_{\pi_f^{-1}(j)} \oplus t_j^{\mathsf{b}_j}]$ and $[\sigma_j^1 = w^1_{\pi_f^{-1}(j)} \oplus t_j^{\bar{\mathsf{b}}_j}]$. P_2 garbles each gate by encrypting the tokens w_c^0, w_c^1 on its outgoing wire with the blinded strings σ_a^0, σ_a^1, σ_b^0, σ_b^1 on its incoming wires according to its truth table. P_2 sends the garbled gates and her garbled input tokens to P_1. P_1 gets his garbled input tokens using OT which can be done in an earlier stage together with other OTs not to increase round complexity. Using the circuit mapping, his blinding strings, the garbled gates and the garbled inputs P_1 evaluates the whole garbled circuit, and obtains the tokens of output bits of $f(x)$. In [6], a gate hiding mechanism is not provided for 2-PFE scheme but instead all gates in the circuit are let to be only a NAND gate.

Mohassel and Sadeghian's scheme involves oblivious evaluation of a switching network made of $2N\mathsf{lg}N + 1$ switches. This is composed of an additional N switches to the ones in their EP construction. The oblivious evaluation of this switching network requires $2N\mathsf{lg}N + 1$ OTs [6]. All of the OTs in the protocol can be combined for just one invocation of OT extension.

[10] For the 1-switches in dummy placement and permutation components, the first and second rows of Table 3 and Table 4, and for 2-switches in replacement components, the second and third rows of Table 3 and Table 4 are sufficient.

4 Our More Efficient 2-Party PFE Scheme

In what follows, we describe our scheme in detail (see also Figure 3).



P_1
P_2
$f \xrightarrow{synt} C_f \xrightarrow{\text{CTH}} (\pi_f, \tilde{C}_f)$
keep π_f private
$\tilde{C}_f$
generate the set:
$T := [t_j \twoheadleftarrow \{0,1\}^\lambda]$
for $j = 1,\ldots,N$
generate the set:
$W^0 := [w_i^0 \twoheadleftarrow \{0,1\}^\lambda]$
for $i = 1,\ldots,M$
join 2-OEP protocol as **Sender**
2-OEP Protocol
join 2-OEP protocol as **Receiver**
receive: $\perp$
receive:
$S^0 := [\sigma_j^0 \leftarrow w^0_{\pi_f^{-1}(j)} \oplus t_j]$
join 2PC protocol as **Evaluator**
2PC Protocol
join 2PC protocol as **Garbler**

Fig. 3. Components and high level procedures of our PFE protocol. The private function f is only known to P_1. P_1 compiles f into a boolean circuit $\mathcal{C}_f$, and extracts the mapping π_f and the template of private circuit $\tilde{\mathcal{C}}_f$. P_1 sends $\tilde{\mathcal{C}}_f$ to P_2. P_1 randomly generates the vector T. P_2 randomly generates the vector W^0. They engage in a 2-OEP protocol where P_2 learns S^0 as the output. With the knowledge of W^0, S^0 and $\tilde{\mathcal{C}}_f$, P_2 garbles each gate and sends the garbled circuit to P_1. With the knowledge of π_f, $\tilde{\mathcal{C}}_f$, T, the garbled circuit and the garbled inputs, P_1 evaluates the whole garbled circuit.

In the preparation stage, P_1 compiles the function into a boolean circuit $\mathcal{C}_f$ consisting of only NAND gates[11], and extract the circuit mapping π_f by randomly assigning incoming and outgoing wire indices. Both party need to have the pre-knowledge of *template of private circuit* $\tilde{\mathcal{C}}_f$ defined as follows:

Definition 4 (Template of Private Circuit ($\tilde{\mathcal{C}}_f$)). *A template of private circuit $\tilde{\mathcal{C}}_f$ is some information about a circuit $\mathcal{C}_f$ which consists of: (1) the number of each party's input bits, (2) the number of output bits, (3) the total numbers of incoming (N) and outgoing wires (M), (4) the incoming and outgoing wire indices which belong to the same gates, (5) the outgoing wire indices corresponding to each parties inputs, and (6) the incoming wire indices belonging to output gates.*

We continue with describing the main parts of our scheme, namely 2-OEP and 2PC garbling protocols. Our complete 2-party PFE protocol is provided in Appendix A.

4.1 Use of 2-OEP protocol

Let w_i^0 and w_i^1 be the tokens for FALSE and TRUE on the ith outgoing wire $\mathsf{ow}_i \in \mathsf{OW}$, respectively, and R be the global free-XOR offset [23] throughout the circuit. P_2 sets $w_i^0 \twoheadleftarrow$

[11] Any functional-complete gate can be used to rule out the need for a gate hiding mechanism as in [6].

$\{0,1\}^\lambda$ for each ow_i. The blinding string on the jth incoming wire $\mathsf{iw}_j \in \mathsf{IW}$ is denoted as t_j. P_1 sets $t_j \twoheadleftarrow \{0,1\}^\lambda$ for each iw_j.

P_1 and P_2 engage in a 2-OEP protocol where P_1's inputs are π_f and a blinding vector for incoming wires $T := [t_j]$ for $j = 1, \ldots, N$, and P_2's inputs is a token vector for FALSE on outgoing wires $W^0 := [w_i^0]$ for $i = 1, \ldots, M$. At the end, P_2 learns the vector of blinded strings for FALSE $S^0 := [\sigma_j^0 = w_{\pi_f^{-1}(j)} \oplus t_j]$ for $j = 1, \ldots, N$, while P_1 learns $\perp$.

Garbler half gate (p_b known to the garbler)	**Evaluator half gate ($p_b \oplus v_b$ known to the evaluator)**
Defines the half gate:	Defines the half gate:
$f_G(v_a, p_b) := (\alpha_1 \oplus v_a)(\alpha_2 \oplus p_b) \oplus \alpha_3$	$f_E(v_a, v_b \oplus p_b) := (\alpha_1 \oplus v_a)(p_b \oplus v_b)$
Computes:	Computes:
$T_{Gc} \leftarrow H(\sigma_a^0) \oplus H(\sigma_a^1) \oplus (p_b \oplus \alpha_2)R$	$T_{Ec} \leftarrow H(\sigma_b^0) \oplus H(\sigma_b^1) \oplus \sigma_a^{\alpha_1}$
$w_{Gc}^0 \leftarrow H(\sigma_a^{p_a}) \oplus f_G(p_a, p_b)R$	$w_{Ec}^0 \leftarrow H(\sigma_b^{p_b})$
Defines the third ciphertext:	
$\psi_c := w_{Gc}^0 \oplus w_{Ec}^0 \oplus w_c^0$	
P_2 sends T_{Gc}, T_{Ec}, and ψ_c.	

Table 5. Adapting half gates technique to our 2-PFE for garbling an odd gate. Here, α_1, α_2 and α_3 define the gate type (*e.g.*, $\alpha_1 = 0$, $\alpha_2 = 0$ and $\alpha_3 = 1$ for a NAND gate, see Equation (2.1)). The token w_c^0 on the output wire equals $w_{Gc}^0 \oplus w_{Ec}^0 \oplus \psi_c$. The three ciphertexts T_{Gc}, T_{Ec}, and ψ_c are sent to P_1 for each gate.

Since our protocol allows all wires in the circuit to have the same offset R, unlike [6], P_1 needs only a single blinding string t_j for each wire, and P_2 does not need to input both tokens w_i^0 and w_i^1 to the 2-OEP protocol. This leads to a considerable decrease in communication cost compared to [6], in which two blinding strings t_j^0 and t_j^1 for each wire are used, and both w_i^0 and w_i^1 are inputs to the OSN protocol (slightly modified 2-OEP protocol).

4.2 Our garbling scheme for 2-PFE

This section presents our garbling scheme based on half gates technique [16]. Similar to half gates technique, P_2 sets $R \twoheadleftarrow \{0,1\}^{\lambda-1}1$, $w_i^1 \leftarrow w_i^0 \oplus R$ for TRUE on each ow_i, and $\sigma_j^1 \leftarrow \sigma_j^0 \oplus R$ for TRUE on each iw_j. We have $\mathsf{lsb}(R) = 1$ so that $\mathsf{lsb}(w_i^0) \neq \mathsf{lsb}(w_i^1)$, and $\mathsf{lsb}(\sigma_j^0) \neq \mathsf{lsb}(\sigma_j^1)$. P_2 follows the steps in Table 5 in order to garble each odd gate.

We now give some necessary notation as follows. Let w_c^0 and w_c^1 denote both tokens on an outgoing wire, while σ_a^0, σ_a^1, σ_b^0, σ_b^1 denote the blinded strings on incoming wires. Let also v_j denote the one bit truth value on the jth incoming wire in a circuit. Further, w_{Gc}^{b} and w_{Ec}^{b} denote the tokens for the garbler and the evaluator half gate outputs for truth value b, respectively. T_{Gc} and T_{Ec} denote the λ-bit strings needed to be sent for the garbler and evaluator half gates, respectively. ψ_c denotes the additional λ-bit string needed to be sent for carrying to the specific output token. w_i and σ_j are the token on ith outgoing wire and the blinded string on jth incoming wire obtained by P_1 while evaluating the garbled circuit, respectively. For the jth incoming wire, let $p_j := \mathsf{lsb}(\sigma_j^0)$ be a value only known to P_2. If two symbols are appended, we imply an AND operation, *i.e.*, $ab = a \wedge b$. $H : \{0,1\}^\lambda \times \mathbb{Z} \to \{0,1\}^\lambda$ denotes a hash function with circular correlation robustness for naturally derived keys, having the security parameter λ.

```
proc $\mathsf{Gb}(1^\lambda, \tilde{C}_f, S^0, W^0)$ :
  $R \twoheadleftarrow \{0,1\}^{\lambda-1}1$
  for $\mathsf{iw}_j \in \tilde{C}_f$ do
    $\sigma_j^1 \leftarrow \sigma_j^0 \oplus R$
  for $\mathsf{ow}_i \in \mathsf{Inputs}(\tilde{\mathsf{C}}_\mathsf{f})$ do
    $e_i \leftarrow w_i^0$
  for each gate $\tilde{G}_i \in \tilde{C}_f$ do
    $\{a, b\} \leftarrow \mathsf{GateInputs}(\tilde{\mathsf{G}}_\mathsf{i})$
    if $\tilde{G}_i$ is a non-output gate then
      $(T_{G_i}, T_{E_i}, \psi_i) \leftarrow \mathsf{Gb}^*_{\mathsf{NAND}}(\sigma_a^0, \sigma_b^0, w_i^0)$
      $F_i^{non-out} \leftarrow (T_{G_i}, T_{E_i}, \psi_i)$
    else
      $(T_{G_i}, T_{E_i}, Y_i^0) \leftarrow \mathsf{Gb}_{\mathsf{NAND}}(\sigma_a^0, \sigma_b^0)$
      $F_i^{out} \leftarrow (T_{G_i}, T_{E_i})$
      $Y_i^1 \leftarrow Y_i^0 \oplus R$
      $d_i \leftarrow \mathsf{lsb}(Y_i^0)$
    end if
return $(\hat{F}, \hat{e}, \hat{d})$

private proc $\mathsf{Gb}^*_{\mathsf{NAND}}(\sigma_a^0, \sigma_b^0, w^0)$:
  $p_a \leftarrow \mathsf{lsb}(\sigma_a^0)$; $p_b \leftarrow \mathsf{lsb}(\sigma_b^0)$
  $k \leftarrow \mathsf{NextIndex}()$; $k' \leftarrow \mathsf{NextIndex}()$
  $T_G \leftarrow H(\sigma_a^0, k) \oplus H(\sigma_a^1, k) \oplus p_b R$
  $w_G^0 \leftarrow H(\sigma_a^0, k) \oplus p_a T_G \oplus R$
  $T_E \leftarrow H(\sigma_b^0, k') \oplus H(\sigma_b^1, k') \oplus \sigma_a^0$
  $w_E^0 \leftarrow H(\sigma_b^0, k') \oplus p_a(T_E \oplus \sigma_a^0)$
  $\psi \leftarrow w_G^0 \oplus w_E^0 \oplus w^0$
return $(T_G, T_E, \psi)$

private proc $\mathsf{Gb}_{\mathsf{NAND}}(\sigma_a^0, \sigma_b^0)$:
  $p_a \leftarrow \mathsf{lsb}(\sigma_a^0)$; $p_b \leftarrow \mathsf{lsb}(\sigma_b^0)$
  $k \leftarrow \mathsf{NextIndex}()$; $k' \leftarrow \mathsf{NextIndex}()$
  $T_G \leftarrow H(\sigma_a^0, k) \oplus H(\sigma_a^1, k) \oplus p_b R$
  $w_G^0 \leftarrow H(\sigma_a^0, k) \oplus p_a T_G \oplus R$
  $T_E \leftarrow H(\sigma_b^0, k') \oplus H(\sigma_b^1, k') \oplus \sigma_a^0$
  $w_E^0 \leftarrow H(\sigma_b^0, k') \oplus p_a(T_E \oplus \sigma_a^0)$
  $Y^0 \leftarrow w_G^0 \oplus w_E^0$
return $(T_G, T_E, Y^0)$
```

```
proc $\mathsf{En}(\hat{e}, \hat{x})$:
  for $e_i \in \hat{e}$ do
    $X_i \leftarrow e_i \oplus x_i R$
return $\hat{X}$

proc $\mathsf{Ev}(\hat{F}, \hat{X}, \pi_f, T)$:
  put $\hat{F}$ in topological order using $\pi_f$
  for $\mathsf{ow}_i \in \mathsf{Inputs}(\hat{F})$ and $j = \pi_f(i)$ do
    $\sigma_j \leftarrow X_i \oplus t_j$
  for each gate $\tilde{G}_i$ {in topo. order} do
    $\{a, b\} \leftarrow \mathsf{GateInputs}(\tilde{\mathsf{G}}_\mathsf{i})$
    $s_a \leftarrow \mathsf{lsb}(\sigma_a)$; $s_b \leftarrow \mathsf{lsb}(\sigma_b)$
    $k \leftarrow \mathsf{NextIndex}()$; $k' \leftarrow \mathsf{NextIndex}()$
    $(T_{G_i}, T_{E_i}, \psi_i) \leftarrow F_i^{non-out}$
    $w_{G_i} \leftarrow H(\sigma_a, k) \oplus s_a T_{G_i}$
    if $\tilde{G}_i$ is a non-output gate then
      $w_{E_i} \leftarrow H(\sigma_b, k') \oplus s_b(T_{E_i} \oplus \sigma_a)$
      $w_i \leftarrow w_{G_i} \oplus w_{E_i} \oplus \psi_i$
      for $j = \pi_f(i)$ do
        $\sigma_j \leftarrow w_i \oplus t_j$
    else
      $(T_{G_i}, T_{E_i}) \leftarrow F_i^{out}$
      $w_{G_i} \leftarrow H(\sigma_a, k) \oplus s_a T_{G_i}$
      $w_{E_i} \leftarrow H(\sigma_b, k') \oplus s_b(T_{E_i} \oplus \sigma_a)$
      $w_i \leftarrow w_{G_i} \oplus w_{E_i}$
      $Y_i \leftarrow w_i$
    end if
return $\hat{Y}$

proc $\mathsf{De}(\hat{d}, \hat{Y})$:
  for $d_i \in \hat{d}$ do
    $y_i \leftarrow d_i \oplus \mathsf{lsb}(Y_i)$
return $\hat{y}$
```

Fig. 4. Our complete half gate based garbling scheme for 2PC. $\mathsf{Gb}_{\mathsf{NAND}}$ and $\mathsf{Gb}^*_{\mathsf{NAND}}$ are the original half gate and our modified NAND garbling procedures, respectively.

Following the framework[12] of [27], Figure 4 depicts our complete garbling scheme, composed of the following procedures. The garble procedure Gb takes 1^λ, $\tilde{C}_f$, S^0 and W^0 as input, and outputs $(\hat{F}, \hat{e}, \hat{d})$ where $\hat{F}$ is the garbled version of $\tilde{C}_f$, $\hat{e}$ is the encoding information, and $\hat{d}$ is decoding information. Gb calls two private gate garbling procedures: (1) $\mathsf{Gb}^*_{\mathsf{NAND}}$ garbles non-output NAND gates, and outputs (T_G, T_E, ψ), (2) $\mathsf{Gb}_{\mathsf{NAND}}$ garbles output NAND gates, and outputs (T_G, T_E, Y^0). En is the encode algorithm that takes the plaintext input $\hat{x}$ of the circuit and e as input, and outputs a garbled input $\hat{X}$. Ev is the evaluate procedure that takes the inputs $\hat{F}$, $\hat{X}$, π_f and T, and outputs garbled output $\hat{Y}$. De is the decode algorithm that takes $\hat{Y}$ and d as input, and outputs the plaintext output $\hat{y}$ of the circuit.

We highlight that the main difference of our garbling scheme from the half gates technique is that the former requires an additional ciphertext ψ_c per gate. This is required because of the nature of 2-PFE, in which the tokens on an outgoing wire are predetermined and specified values, while in the in half gates they are indeed a function of the input strings. Since in our scheme the output tokens of output gates are not predetermined, these gates can be garbled with half gates technique. Each output gate is then garbled with two ciphertexts.

Note also that P_1 gets his own garbled inputs by means of OT. This can also be done in an earlier stage together with other OTs in 2-OEP protocol (if OSN construction is used) in order not to increase round complexity. For this setting, P_2 needs to pick R and compute the tokens for TRUE on P_1's input wires before 2-OEP protocol. This setting is compatible with our protocol as well.

```
{modify the antepenultimate line of Gb}
 $k \leftarrow \mathsf{NextIndex}()$; $d_i \leftarrow (H(Y_i^0, k), H(Y_i^1, k))$
```

```
proc $\mathsf{De}(\hat{d}, \hat{Y})$:
  for $d_i \in \hat{d}$ do
    $k \leftarrow \mathsf{NextIndex}()$; parse $(h_0, h_1) \leftarrow d_i$
    if $H(Y_i, k) = h_0$ then $y_i \leftarrow 0$
    else if $H(Y_i, k) = h_1$ then $y_i \leftarrow 1$
    else return $\perp$
  return $\hat{y}$
```

Fig. 5. Modification of our garbling scheme in Figure 4 for achieving authenticity property defined in [27].

4.3 Security of the proposed protocol

Security of our protocol basically relies on the main line of the security proofs in [5, 6].

			MS'13 [6]		**Our Protocol**	
			No. of Strings	**String Length (bits)**	**No. of Strings**	**String Length (bits)**
OSN	**Before OT Ext.**	$P_2 \to P_1$	N	2λ	N	λ
	During OT Ext.	$P_1 \to P_2$	λ	$2N\lg N + 1$	λ	$2N\lg N - N + 1$
		$P_2 \to P_1$	$4N\lg N - N + 2$	2λ	$4N\lg N - 2N + 2$	λ
	After OT Ext.	$P_1 \to P_2$	N	2λ	N	λ
2PC	**Garbled Circ.**	$P_2 \to P_1$	$2N$	λ	$1.5N$	λ
TOTAL (bits)			$(10N\lg N + 4N + 5)\lambda$		$(6N\lg N + 0.5N + 3)\lambda$	

Table 6. Analysis of communication costs for 2-party PFE schemes (see Section 3.1 for details of transfers in the OSN phases).

[12] Bellare, Hoang, and Rogaway introduce the notion of a garbling scheme as a cryptographic primitive. They also describe procedures and security requirements of garbling schemes. We refer the reader to [27, 28] for details concerning definitions and introduction to the formal concepts of garbling schemes.

Theorem 1. *Given that the 2-OEP protocol used in our protocol is secure in presence of semi-honest adversaries, and that our garbling scheme based on half gates technique uses a hash function H with circular correlation robustness for naturally derived keys [16], then our two party PFE protocol is secure in the presence of semi-honest adversaries.*

Proof sketch. In accordance with [5,6], we divide our scheme into two phases: (1) generation of random strings the wires of each gate (via 2-OEP protocol), (2) execution of Yao based 2PC scheme (via our half gates based protocol) using those strings. In the first phase, we utilize the 2-OEP protocol in a black-box manner. The second phase esentially utilizes our half gates based garbling. Under the following two conditions, the security of our protocol depends on the security of half gates garbling scheme against semi-honest adversaries:

1. The collection of $3g - o$ λ-bit strings used in garbling (*i.e.*, $2g$ for FALSEs on gate inputs and $g - o$ for FALSEs on non-output gate outputs) must be indistinguishable to P_2 from a uniformly random distribution $\mathsf{U}_{(3g-o)\lambda}$.
2. P_1 cannot have any further knowledge other than a specific linear constraint set between a subset of keys (the tokens on the outgoing wires and the blinded strings on the incoming wires). This set of constraints cannot provide any advantage to obtain any key values.

In [6], it is shown that the first phase of the 2-PFE meets the two conditions mentioned above for the set of generated keys. Hence, the security of our overall protocol relies on the security of our half gates based garbling scheme. In what follows, we provide a reduction to the security of half gates technique which is already proven in [16].

The main difference of our garbling scheme from [16] is the additional third ciphertext ψ_i for each garbled non-output gate. ψ_i is the linear constraint between the output token of a non-output gate (w_i) which is chosen uniformly at random and the half gate output tokens (w_{Gi} and w_{Ei}) whose value depends on the input blinded strings. In P_1's view, who does not have any pre-information about w_i, ψ_i is indistinguishable from U_λ due to the security characteristics of one-time pad encryption. Hence, ψ_i does not give any information about the input tokens of the gate. Therefore, the security of our scheme is reduced to half gates technique in terms of privacy and obliviousness [27].

Since ψ_i is not included in an output gate, it does not affect authenticity of half gates garbling. In accordance with [16], our garbling scheme in Figure 4 can be modified as in Figure 5 to achieve authenticity property [27].

5 Complexity Analysis

We analyze the complexity of our protocol, and compare it with Mohassel and Sadeghian's 2-party PFE scheme [6]. Without loss of generality, in order for a fair comparison, we assume that the 2-OEP protocol of our scheme is also realized by the OSN construction in [6], and that the OSN phases in both protocols are optimized with the General OT extension scheme of Asharov, Lindell, Schneider, and Zohner [21]. Similar results can be obtained by using other Ishai *et al.* based OT extension schemes [19, 20] as well.

Regarding the OSN phase, the total number of OTs in our 2-PFE protocol is $2N\lg N - N + 1$, while it is $2N\lg N + 1$ in [6] (see Section 3.1). Moreover, our protocol requires only one of the tokens on a wire entering the OSN phase, so the size of the rows in Table 4 which enter each OT is reduced by a factor of two [6], further resulting in a significant decrease in communication cost.

Regarding the 2PC phase, our scheme garbles each non-output gate with three ciphertexts, and each output gate with two ciphertexts. This yields more than 25% reduction compared to the same phase in the scheme in [6].

No. of	MS'13 [6]			Our Protocol			Overall
Gates	OSN Phase	2PC Phase	Total	OSN Phase	2PC Phase	Total	Reduction
2^8	47,109	1,024	48,133	27,139	768	27,907	42.0%
2^{10}	229,381	4,096	233,477	133,123	3,072	136,195	41.7%
2^{12}	1,081,349	16,384	1,097,733	630,787	12,288	643,075	41.4%
2^{14}	4,980,741	65,536	5,046,277	2,916,355	49,152	2,965,507	41.2%
2^{16}	22,544,389	262,144	22,806,533	13,238,275	196,608	13,434,883	41.1%
2^{18}	100,663,301	1,048,576	101,711,877	59,244,547	786,432	60,030,979	41.0%
2^{20}	444,596,229	4,194,304	448,790,533	262,144,003	3,145,728	265,289,731	40.9%

Table 7. Communication cost comparison of 2-party PFE schemes in terms of λ bits.

Table 6 shows the number of strings and their corresponding lengths sent in each turn in both schemes (see also Section 3.1 for details of transfers in the OSN phases). We omit the OTs for P_1's garbled input, the transfers for decoding the garbled output, and the base OTs in the OT extension scheme [21]. The strings sent by P_2 during the OT extension in [6], in fact, consists of $4N\lg N - 2N + 2$ of λ-bit stings and $2N$ λ-bit strings. The data sent by P_2 before OT extension can also be sent during P_2's turn in OT extension for a saving in the number of rounds.

Table 7 reflects the communication cost reduction resulting from our 2-PFE protocol for various gate number levels including 2^6, 2^{10}, 2^{14}, 2^{18}, and 2^{20}.

Recently, in [13], Wang and Malluhi attempt to improve the 2-PFE scheme in [6] by removing only one ciphertext from each garbled gate while remaining the cost of OSN phase unchanged. However, the influence of 2PC phase in [6] on overall communication cost is already quite low (see Table 7). Reducing the bandwidth use in the 2PC phase by 25% only results in less than 1% reduction in the total cost. For instance, given a circuit with 1024 gates, their optimization reduces the communication cost of the 2PC phase from 4,096 λ-bit strings to 3,072 of them, while the OSN phase cost remains 229,38 λ-bits. Therefore, the overall gain from their optimization for this setting is $\sim$0.4%.

Besides the bandwidth improvements, our protocol also slightly enhances [6] in terms of computation complexity. In 2PC phase, our scheme requires an additional cryptographic operation per gate in Ev procedure compared to the garbling scheme in [6], resulting in additional $0.5N$ operations in total. On the other hand, our protocol requires N-less OTs in OSN phase, resulting in $2N$-less symmetric encryptions by P_2, assuming that the smaller input strings to an OT does not change the cost of the cryptographic operations involved. In fact, these are asymptotically low costs compared to the total computation requirements of both schemes since both require $O(N\lg N)$ cryptographic operations.

The round complexity of our scheme does not differ from the 2-PFE scheme in [6] since our protocol still consists of a constant round OT extension scheme in OSN phase, and our half gate based garbling scheme in 2PC phase consists of the same number of rounds as in the basic garbling scheme used in [6].

6 Conclusion

In this paper, we proposed an efficient and secure protocol for 2-PFE. The motivation behind our work is that the bandwidth of various channels is the main constriction for many secure computation applications, including the ones for PFE. Our optimization significantly improves Mohassel and Sadeghian's 2-PFE scheme [6] in both OSN and 2PC phases in terms of communication complexity. In particular, in OSN phase, our protocol reduces the number of required OTs and data sizes entering the protocol. In 2PC phase, our half gate based scheme garbles each non-output gate with three ciphertexts, and each output gate with two ciphertexts. All in all, our protocol improves the state-of-the-art by saving more than 40% of the overall communication cost.

We conclude with the following two open questions:

1. Although the 2-OEP protocol in [6], which we utilize in our protocol, is quite efficient for many circuit sizes, fails to be so in large-sized circuits due to its $O(g\lg g)$ complexity. This fact arises the following question: *Can we have a 2-OEP protocol that has linear asymptotic complexity while also being efficient in small circuit sizes?*
2. Our 2-PFE protocol permits only one gate functionality (*e.g.*, NAND or NOR) in a boolean circuit. This yields another important future challenge: *Can we have a gate hiding mechanism in 2-PFE schemes permitting the use of various gates in logic circuit representations?*

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A Our Complete 2-Party PFE Protocol

Our 2-PFE(f, x_1, x_2) Protocol

P_1**'s Input:** A bit string x_1 and a function f.
P_2**'s Input:** A bit string x_2.
Output: $f(x_1, x_2)$.

Preparation:

1. P_1 compiles the private function $f(x_0, x_1)$ into a boolean circuit $\mathcal{C}_f$ whose the number of input bits, output bits, and gates are n, o, and g, respectively, extracts the mapping π_f by randomly assigning incoming and outgoing wire indices, and prepare the template of private circuit $\tilde{\mathcal{C}}_f$.
2. P_1 sends $\tilde{\mathcal{C}}_f$ to P_2.
3. P_2 randomly generates an λ-bit token $w_i^0 \twoheadleftarrow \{0,1\}^\lambda$ for FALSE on each $\mathsf{ow}_i \in \mathsf{OW}$. This yields a total of $M = n + g - o$ pairs. Moreover, P_2 sets a vector $W^0 := [w_i^0]$ for $i = 1, \ldots, M$.
4. P_1 generates an λ-bit blinding string $t_j \twoheadleftarrow \{0,1\}^\lambda$ for each $\mathsf{iw}_j \in \mathsf{IW}$. He sets those values to a blinding vector $T := [t_j]$ for $j = 1, \ldots, 2g$.

2-OEP Protocol:

5. P_2 and P_1 engage in a 2-OEP protocol where P_1's inputs are the mapping π_f and T, while P_2's input is the vector W^0. At the end, P_2 learns the blinded string vector $S^0 := [\sigma_j^0 = w_{\pi_f^{-1}(j)} \oplus t_j]$ for $j = 1, \ldots, N$, while P_1 learns $\perp$.

Yao's Protocol (P_2 **becomes the garbler, and** P_1 **becomes the evaluator):**

6. **Garbling:** P_2 generates a secret λ-bit offset $R \twoheadleftarrow \{0,1\}^{\lambda-1}1$. P_2 sets the token for TRUE on each ow_i as $W_i^1 \leftarrow W_i^0 \oplus R$, and the blinded for TRUE on each iw_j as $\sigma_j^1 \leftarrow \sigma_j^0 \oplus R$. Moreover, P_2 sets the sets $W^1 := [w_i^1]$ for $i = 1, \ldots, M$ and $S^1 := [\sigma_j^1]$ for $j = 1, \ldots, N$. With the knowledge of W^0, S^0, S^1 and $\tilde{\mathcal{C}}_f$, P_2 garbles each odd gate using the Gb procedure in Figure 4, resulting in three ciphertexts per non-output gate and two ciphertexts per output gate. P_2 sends the garbled circuit $\hat{F}$ and the tokens for her own inputs to P_1. P_1 gets tokens for his own input bits from P_2 using 1-out-of-2 OTs. (If OSN construction is used, these OTs can be jointly executed with the ones for 2-OEP protocol in parallel and with just one invocation of extended OT. For this setting, P_2 needs to pick R and compute the tokens for TRUE on P_1's input wires before 2-OEP protocol.)
7. **Evaluating:** With the knowledge of π_f, T, $\hat{F}$ and the garbled input $\hat{X}$, P_1 evaluates the whole garbled circuit in topological order. When an outgoing wire i is mapped to an incoming wire j, the token w_i is XORed with t_j to reach the blinded string σ_j. P_1 evaluates each garbled gate using the Ev procedure in Figure 4. At the end, P_1 reaches the tokens of output bits of $f(x_0, x_1)$.

Fig. 6. Our 2-Party Private Function Evaluation Protocol