

Key Extraction from the Primary Side of a Switched-Mode Power Supply

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Abstract. In this paper we detail techniques that can be used to analyze and attack an AES implementation on an FPGA from the primary (i.e., external) side of a switched-mode power supply. Our attack only requires measurements of the duty cycle of the power supply, and then increases the signal-to-noise ratio (SNR) through averaging, deconvolution and wavelet based detrending. The result is an exploitable source of leakage that allows a secret key to be determined from low-frequency power measurements. The techniques and procedures provide a general approach to performing differential power analysis (DPA) from a single point of information for any single hypothesized intermediate value, suggesting their potential for improving other types of side-channel analysis.

Keywords: Side-Channel Analysis, DPA, Switched-Mode Power Supply, Deconvolution, Detrending, Wavelets

1 Introduction

Side-channel analysis was first proposed as a method of extracting cryptographic keys by Kocher [11], who noted that the time required to compute an RSA signature could reveal a private key. Further work demonstrated that one could determine cryptographic keys by observing the power consumption over time [12]. Two types of attacks were proposed. The first was inspecting a single power consumption trace, referred to as Simple Power Analysis (SPA), and a statistical treatment of a set of traces, referred to as Differential Power Analysis (DPA). It was later shown that one could use the same treatment on traces taken using electromagnetic probes [7, 16], where the equivalent attacks are typically referred to as Simple Electromagnetic Analysis (SEMA) and Differential Electromagnetic Analysis (DEMA), respectively. With adequate sampling rates, proximity, and absence of countermeasures, side-channel attacks have been practically demonstrated on a wide variety of devices ranging from small single purpose chips [2, 6, 10] to large general purpose SoCs and CPUs [8, 15, 19].

If we consider an implementation of a cryptographic algorithm in a tamper resistant enclosure, one could assume that no meaningful power or electromagnetic measurements can be made. While examples of such metal cases that leak

information are present in the literature [8], we shall assume that this avenue of attack is not available to an attacker. Alternatively, an attacker could try to determine the power consumption of the entire device by focusing on the external power supply. For example, the primary (i.e., external) line of the internal switched-mode power supply (SMPS) that supplies its internal components. The nature of an SMPS means that its power consumption over time is not directly correlated with the power consumption of a device it is powering. One might assume that the combination of a secure enclosure and an SMPS would be sufficient to protect a device from side-channel analysis.

In this paper, we describe a key extraction attack only using duty cycle information taken from the primary side of an SMPS, where the measurements reduce the information from a trace to a single value that summarizes the leakage for a period of time. We show how leakage can be detected and then exploited to allow cryptographic keys to be retrieved. We provide experimental results showing how our attack can be applied at some distance from the device, i.e. an attacker does not need direct access to a device, but could, for example, monitor it from a wall-mounted transformer. In the first results we describe, we show how a straightforward DPA can be applied using a moderately large number of acquisitions. We then demonstrate how acquisitions can be treated using wavelets to improve the signal-to-noise ratio in our acquisitions, significantly reducing the number of acquisitions required to conduct our attack. We conclude with some discussion of how these methods could also be applied to other types of side-channel analysis.

The remainder of this paper is organized as follows. In Section 2 we describe how a switched-mode power supply operates, why leakage is visible on the primary side of the power supply, and the basic phenomenon that allows one to detect power usage on its secondary side. In Section 3, we describe how we can validate the efficacy of different measurement techniques and how to work around the constraints imposed on how we measure power usage on the secondary side of an SMPS from its primary side. In Section 5, we discuss results on validating the efficacy of the proposed measurement techniques. In Section 5, we discuss results on performing a key extraction using the proposed measurement technique in addition to other signal processing techniques required to make the attack successful. We conclude in Section 6.

2 Switched-Mode Power Supplies

Switched-mode power supplies (SMPS) have gained popularity over the past 35 years because of their efficiency, low operating temperature and size (when compared to other power supplies such as linear regulators). Their efficiency stems from their switching characteristic, when operating an SMPS will repeatedly connect and disconnect the input, or primary, to the load, or secondary, to power a device. Many SMPS configurations have been developed to achieve various performance characteristics. By modulating the width of a pulse of the full input voltage, and low-pass filtering that pulse, an SMPS can control the sec-

ondary voltage level and adjust according to changing load characteristics. The trade-offs associated with using an SMPS include a more complex design and high-amplitude, high-frequency voltage spikes caused by switching. The injected voltage spikes on the power line need to be filtered, adding further complexity.

The nature of an SMPS might lead one to conjecture that power measurements from its primary side contain only minimal information about the power consumed on its secondary side. One attack strategy might be to integrate over time a measurement of power on the primary side, and incorporate an accurate efficiency characterization of the SMPS, to approximate the energy consumed on the secondary side. Yet another argument could state that the ground, or return line, on the primary side, never disconnects from the secondary side, hence measuring the return power on the primary side could contain power usage information from the secondary side, albeit with reduced resolution because of the required capacitance on the primary side.

While the above arguments do not allow for effective DPA-based key extraction in practice, monitoring the return line has been demonstrated to expose leakage with potential to extract keys in low-noise environments. High-amplitude, high-frequency spikes on the input lines, that typically manifest as noise in a side-channel attack, nonetheless provide power usage information through their locations in time. Furthermore, given that the spikes are high in amplitude and frequency, they can be observed through noisy environments, filtering, over distance, and through shielding.

2.1 Voltage Spike Interpretation and Detection

When operating, an SMPS generates voltage spikes on its primary side. The cause of these voltage spikes stem from a combination of the fundamental mode of operation of an SMPS, and unavoidable practical physical attributes found in all electrical circuits (specifically, switching and inductance). SMPS switching causes sudden changes in current flow through parasitic inductance of the circuit that, in turn, induces a voltage. The magnitude of the induced voltage follows the relationship

$$V(t) = L \frac{dI(t)}{dt} ,$$

where V is voltage, t is time, L is inductance and I is current. Obviously, a sudden change in current, such as the switching from an SMPS, generates a very large multiplier applied to the inductance that in turn generates a very large induced voltage spike.

While electrical circuits contain parasitic inductance, a major contributor to the inductance responsible for inducing voltage spikes on the primary side comes from the required capacitance on the primary side, which is used to quickly provide current when the SMPS switches on. The equivalent series inductance of the resulting capacitor becomes part of the circuit that passes the sudden inrush and sudden stops in current. Figure 1 shows a common electrically equivalent model of a capacitor with its parasitic contributors.

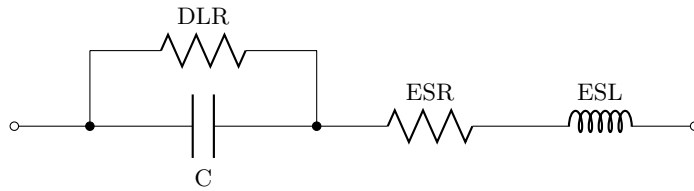


Fig. 1. Electrical model of capacitor where C is the capacitance, DLR is the dielectric leakage resistance, ESR is the equivalent series resistance, ESL is the equivalent series inductance.

Figure 2 shows a sample voltage signature of a tapped power source feeding an SMPS. At the beginning of each spike, the voltage either suddenly dips or rises, followed by ringing due to the resonance of the circuit feeding the SMPS. The tapped line connects to a high-pass filter before connecting to an oscilloscope to remove the DC bias and any ripple caused by the SMPS. From the direction of the initial peak, one can easily identify the first spike as an on event and the second spike as an off event. One can also notice the magnitude difference, allowing an oscilloscope trigger to be set on either an on or off event. We describe why some of these differences occur in Appendix A.

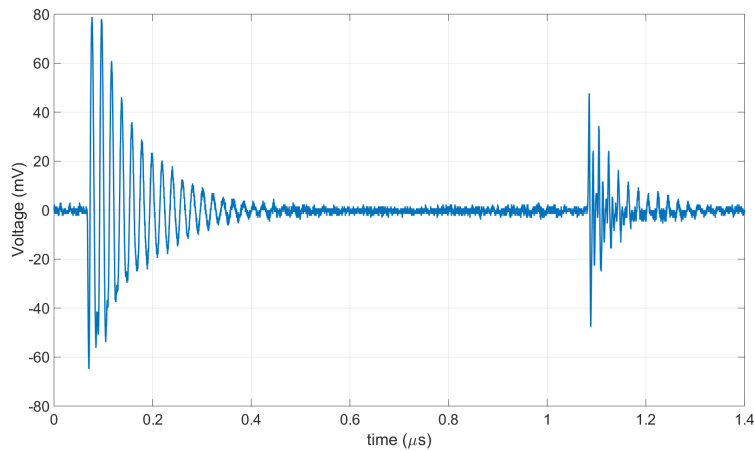


Fig. 2. Voltage trace on primary side of an SMPS showing an on event followed by an off event.

3 Leakage Detection

A powerful approach for determining if the power consumption of a device relates to the data it is manipulating, referred to as Test Vector Leakage Assessment (TVLA), has been proposed by Goodwill et al. [9]. In summary, TVLA uses a t -test to evaluate leakage from comparing acquired signals when a device is processing specific inputs and/or cryptographic keys, which provides a clear indication of leakage.

One of the tests in TVLA is to determine whether there are statistically significant differences in the mean traces of two sets of traces, one acquired with a fixed plaintext and the other with random plaintexts. One would typically randomly interleave acquisitions so that environmental effects are the same for both sets and there are no erroneous indications of leakage, caused, for example, by the least significant bit of a variable used to count the number of acquisitions. In applying this, one would take two sets of data, and conduct Welch’s t -test point-by-point to determine whether there is evidence against the null hypothesis that the sets are the same.

Consider two sets of acquisitions, of n_1 and n_2 samples, respectively. We can compute their respective sample means, \bar{x}_1 and \bar{x}_2 , and respective sample standard deviations, σ_1 and σ_2 . One can then compute a t -statistic using Welch’s t -test

$$\alpha = \frac{\bar{x}_1 - \bar{x}_2}{\sqrt{\frac{\sigma_1^2}{n_1} + \frac{\sigma_2^2}{n_2}}}, \quad (1)$$

where the result is distributed over a t -distribution with ν degrees of freedom, i.e., $\alpha \sim t(\nu)$. In practice, one would use the asymptotic result where the t -distribution is equivalent to the standard normal distribution, so ν does not need to be defined.

Goodwill et al. propose that observing $\alpha > 4.5$ indicates the presence of leakage. Specifically, an $\alpha > 4.5$ gives the probability of indicating leakage where no leakage is present, often referred to as a Type I error, of approximately 1×10^5 . However, repeating an experiment can mitigate this problem. The probability of no leakage being indicated where leakage is present, often referred to as a Type II error, is not defined but, again, repeating an experiment can mitigate this problem. To detect side-channel leakage that could be used to conduct an attack, one would typically use this test on a set of power consumption traces where the t -statistic is computed in a point-wise manner. That is, one can test for leakage at each point in time using two sets of acquisitions.

In our case, large portions of a cryptographic operation can affect a single on-off switching period because of the low-frequency content of the SMPS duty cycle. Indeed, depending on the algorithm and SMPS, the execution of an entire block cipher, or multiple instances of a block cipher, including input and or output data can all affect a single SMPS duty cycle. If one were to compare the power usage between a set of random inputs and a set of fixed inputs, as described by Goodwill et al. [9], power dependencies attributed to the input and output data would add together with other leakages, making it impossible to

determine if exploitable leakage is present. The multi-dimensional, but single-point, result of translating power usage on the secondary side of an SMPS to its duty cycle requires the use of targeted vectors, similar to the approach described by Mizaki and Hayashi [14].

To construct a TVLA-like test for leakage detection we target the middle of a cryptographic operation, while having inputs and outputs that are indistinguishable from random values via some side-channel. For example, to evaluate an AES encryption operation one would target a middle round of the block cipher. For that round, the round key and state maintain a minimal Hamming distance between the input and output and low Hamming weight of both states. We give further details on how we constructed the required plaintexts in Appendix B.

The resulting set of plaintexts can be randomly interleaved with random plaintexts to provide a good method of detecting leakage using the methods described by Goodwill et al. The test accentuates any leakage caused by Hamming weight or Hamming distance in the implementation of a round of AES. We note that a specific secret key must accompany the plaintexts, so such a test requires the ability to set the secret key in the targeted device. Furthermore, if this version of TVLA reveals a leak, the results do not specifically reveal a particular type of leak, or indicate how to exploit the leakage to determine a secret key. However, by using the same technique, one can generate more specific plaintexts, with associated secret keys, to help isolate where and how a leakage manifests.

4 Attacking the Primary Side of an SMPS

In this section we describe an instance of our attack, and how to detect and exploit the observed leakage to extract cryptographic keys. In our instance, we targeted a SASEBO-GII [17] where the on-board FPGA was powered by an SMPS, and the only side-channel that we observed was the primary side of the SMPS. Table 1 provides the specifications of the SASEBO-GII and associated SMPS. The SMPS sets its output voltage based on a connected resistor R_{SET} . An R_{SET} of 27.4 Ohms was used to set the SMPS output to 1.2 Volts. The SMPS was then configured to mate with the CN1 connector on the SASEBO-GII board, providing power to the FPGA core. The sense resistors R1 and R2 were bypassed, and the resulting voltage between test points TP2 and TP4 was 1.17 Volts. The AES implementation used was the reference design provided with the SASEBO board.

4.1 Leakage Detection

The first experiments we conducted were to determine how leakage occurred and how it could be exploited. For a series of AES encryption operations, the input to each operation was randomly chosen as either a targeted or random plaintext using the method described in Section 3. An oscilloscope was used to acquire a voltage trace from the source powering the SMPS, and a trigger was included in our implementation such that we could take acquisitions while

Table 1. SASEBO-GII and associated SMPS

SASEBO-GII	
FPGA	Xilinx Virtex 5 LX50
Algorithm	AES-128

SMPS Providing Power to FPGA Core	
Manufacturer	Texas Instruments
Part Number	PTH08000W
Input Voltage Range	4.5 Volts – 14 Volts → set to 4.5 Volts Input
Output Voltage Range	0.9 Volts – 5.5 Volts
Switching Frequency	300 kHz
Input Capacitor	100 uF Electrolytic
Set Resistor (R_{SET})	27.4 kOhms Metal Film → 1.2 Volts Output

the AES was being computed. Predictably, the SMPS switching events did not synchronize with the AES encryption execution. However, any load variation on the SMPS secondary side can only affect subsequent duty cycles of the SMPS, so the oscilloscope was set to collect a trace long enough to record multiple duty cycles after the AES encryption operation. Initially, over 25 cycles were recorded. Analyzing the differences in the time between on and off events one could readily observe a t -statistic larger than 4.5.

To exploit this leakage, one could further treat the acquired data to maximize the observed leakage. For example, if we let

- c = number of duty cycles directly after trigger,
- \mathbf{w} = weight vector of c elements, and
- d = delay after trigger before first on event.

Then we use c determined the number of duty cycles to process in each trace, \mathbf{w} for the weight of each duty cycle, and d as a maximum delay threshold before excluding a trace and its associated data. For each acquired trace, if less than d , a \mathbf{w} weighted sum of c duty cycles provided a single number representing a relative power draw of the load.

Using targeted vectors, as described in Section 3, we collected a total of 1.3×10^5 traces comprising approximately 2^{16} targeted inputs and 2^{16} random inputs. Setting $d = 2.08 \mu\text{s}$ reduced the targeted and random sets to approximately 4×10^4 traces. Setting $c = 4$ and $\mathbf{w} = [0.91 \quad -0.41 \quad 0.027 \quad -0.071]^T$ on the reduced sets, (1) gave a t -statistic of 18.58, yielding a confidence level of $1 - 5.639 \times 10^{-71}$ that the measured duty cycles reflect a change in cryptographically sensitive information within an AES encryption operation. This provides insight into how this side channel leaks since, for this instance, every other cycle is inversely correlated to the leakage.

Variants of the above approach can be considered, such as setting a threshold to determine inclusion for each duty cycle within each trace and weighting appropriately, or setting an early threshold for duty cycles that potentially rep-

resent too much activity before an AES encryption operation, etc. However, the approach described in the next section provides a more substantial increase to the t -statistic, allowing our analysis to move from leakage detection to extracting a secret key.

4.2 Improving the Signal-to-Noise Ratio

The experiments described in Section 4.1 provided confidence that measuring duty cycles from the primary side of an SMPS can expose leakage from a device on the secondary side. In order to strengthen the coupling between the SMPS duty cycle and the power required to encrypt a specific input, we repeatedly sent the same message to the AES engine. This also allowed us to trigger an oscilloscope when an SMPS event occurred, as we no longer needed know when an individual AES encryption operation was occurring. Furthermore, rather than measuring the full duty cycle from a recorded voltage trace, the triggered on event was shifted to allow only the off event to be recorded with a high time resolution. Given that this provided a fixed reference in time for the on event, an oscilloscope could generate an average trace on-the-fly to provide an average location of the off event.

Using on-scope averaging allows one to process a large amount of data in a short period of time by removing the time required to transfer individual acquisitions to a computer. The larger the number of traces that are averaged, the greater the efficiency, at the cost of a lower number of unique inputs. The low frequency information of the SMPS duty cycle translates to convolving high frequency leakage information on the secondary side with temporal noise. Hence, on-scope averaging has the potential to provide improvements in increasing a t -statistic in a fixed amount of time.

Our first experiments incorporated a low-pass filter in an attempt to increase the voltage spike oscillation period, so that it is greater than the duty cycle jitter. With such a signal, the average voltage trace converges faster because there are fewer interfering voltage oscillations after the initial spike. Figure 3 shows a single low-pass filtered signal. Figure 4 shows the beginning of 100 off events at a higher time resolution with the mean off event superimposed.

Performing the leakage detection techniques, as described in Section 4.1, substituting the weighted sums of duty cycles with mean off events yielded a t -statistic of 92.88σ . Figure 5 shows the resulting means of the two sets and the resulting t -statistic over time. At this point we had enough confidence to perform an key recovery attack based on the observed side channel.

5 Side-Channel Attack on Primary Side of SMPS

In order to construct a key extraction attack one would typically need to try different sets of plaintexts to reveal leakage corresponding to specific leakage models (as described in Appendix B). Determining a leakage model would facilitate an attack. However, one may alternatively make an educated guess and

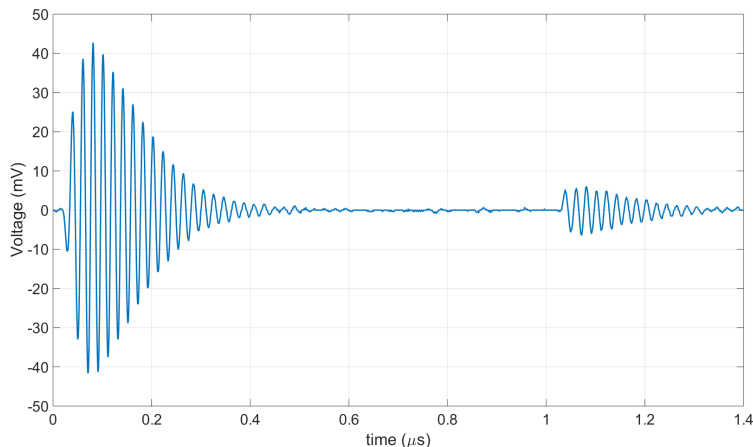


Fig. 3. Low frequency content of Voltage trace on primary side of SMPS.

attempt an attack. In the case of the SASEBO-GII, the intermediate states that leak correspond to a leakage model that had already been determined, given our knowledge of the FPGA. As such, we conducted an attack using correlation power analysis (CPA) [3] on the Hamming distance across the last round of the AES encryption operation. In common with many hardware implementation, the reference AES implementation provided with the SASEBO board updates a register at the end of each round of AES. The Hamming distance between the output of two consecutive rounds affects the power consumption of the FPGA when this register is update. Using the data collection method described in Section 4.2, 1.85×10^5 unique inputs were required to extract only one byte of the last subkey. In the following we describe additional signal processing approaches that were used decrease the number of traces required to conduct an attack.

5.1 Wavelet Based Detrending

Inspecting our analysis of the duty cycles over time revealed a large drift, which reduces the SNR in a set of acquisition. The observed drift could be caused by many factors, such as temperature and other physical forces that affect the electrical characteristics of the load perceived by the SMPS. However, the source of the drift is beyond the scope of this paper. To increase the SNR we used detrending techniques before applying a CPA, specifically the discrete wavelet transform (DWT) [13].

The scaling and wavelet coefficients used were the Daubechies family of wavelets [4]. The reason for using the DWT with the Daubechies wavelets stems from the desire to preserve the relative change in mean duty cycle as much as possible, while removing any drift that can changes slowly and/or quickly. The Daubechies wavelets provide the maximum number of vanishing moments for a

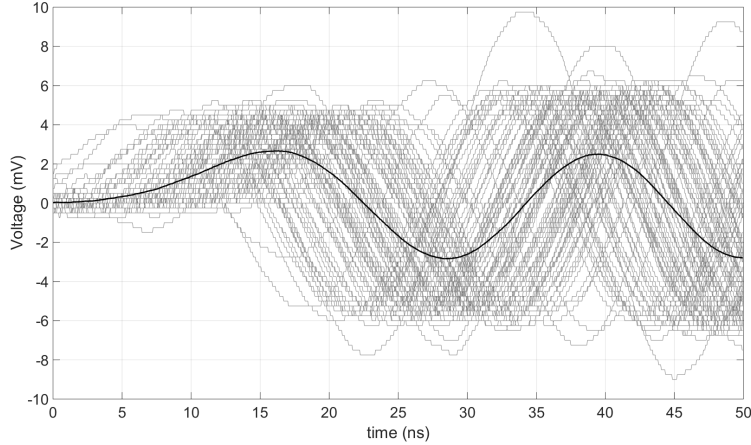


Fig. 4. One hundred off switching events and their mean.

given support, which translates to the flattest frequency response of the filters used in the DWT for a given number of taps [4]. The flatter the frequency response in the band of interest, the more preserved the duty cycles remain when transformed. The fewer taps used in the filters, the faster the DWT can respond to sudden duty cycle drifts. The accuracy of approximation of a signal $f(t)$, represented at a resolution j , or $f_j(t)$, follows

$$\|f(t) - f_j(t)\| \leq C2^{-jp}\|f^{(p)}(t)\| \quad \text{and} \quad \int_{-\infty}^{\infty} f(t)w_{jk}(t)dt \leq C2^{-jp}$$

where C is a constant dependent on the scaling and wavelet functions, and p is the number of vanishing moments of the wavelet function (or number of zeros at π of the DWT approximation filter) [4, 18]. Figure 6 shows the frequency response of the DWT filters when using Daubechies wavelets with $p = 2$ and $p = 8$, or db2 and db8, respectively. A compromise exists because the number of taps is equal to double the value of p . So the better the fit, the less reactive the DWT becomes to sudden changes in duty cycle drift.

The detrending technique follows a simple algorithm, inspired by the wavelet shrinkage techniques as described in [5]. Perform the DWT, or analysis, with a chosen filter order for an L number of levels. Set all of the resulting approximation coefficients to zero, then perform an inverse DWT, or synthesis, on the remaining detail coefficients. Further enhancements could be made by performing thresholding (akin to that described in [5]), but on the scaling rather than detail coefficients.

After detrending the signal using the above method with various ordered filters at various levels, we were able to extract the last round key with 1.25×10^5 unique inputs over 4 days. However, each unique trace comprised of 2^{16} averaged

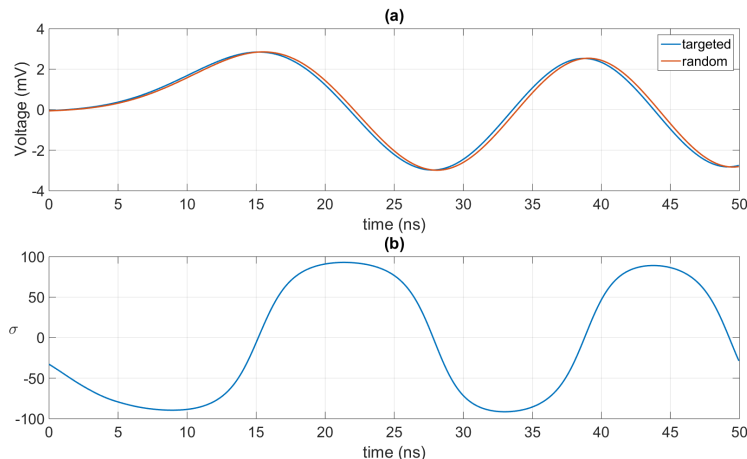


Fig. 5. Plot (a) shows the mean of the two sets of mean off events: targeted and fixed. Plot (b) shows the resulting t -statistic.

traces. Using the same data without detrending, we could only extract one sub-byte from the last round key. In general analyzing 2 – 4 levels with various ordered filters worked well, but 3 levels provided the best consistent results. Figure 7 shows the typical duty cycle drift observed before and after detrending.

5.2 Deconvolution

The next approach we used to increase the SNR of the measured duty cycles focused on a more accurate PDF of the off events mean. The method follows a straightforward deconvolution, by observing that a waveform shifted and added to itself maps to a phase change in the frequency domain. The property comes directly from the linearity and time shifting properties of the Laplace, Fourier and z transforms [1]. For the z transform,

$$\mathcal{Z} \left[\frac{1}{M} \sum_{m=0}^{M-1} f(nT + k_m T) \right] = \frac{1}{M} \sum_{m=0}^{M-1} z^{k_m} \mathcal{Z} [f(nT)] ,$$

where $f(nT)$ is a single off event waveform, T is the sampling period, M is the number of off events averaged, and $\mathbf{k} = [k_0 \ k_1 \ \dots \ k_{M-1}]^T$ is a vector of samples that the m^{th} off event is shifted relative to $f(nT)$.

The deconvolution technique follows a straightforward series of steps. First, we align a collection of single off event waveforms to generate a low-noise template $f(nT)$. Take a series of single off event waveforms and average them without alignment. Divide the frequency response of the averaged non-aligned waveforms by the frequency response of the template, and calculate the group delay of the resulting spectrum. One then seeks to identify frequencies that consistently and

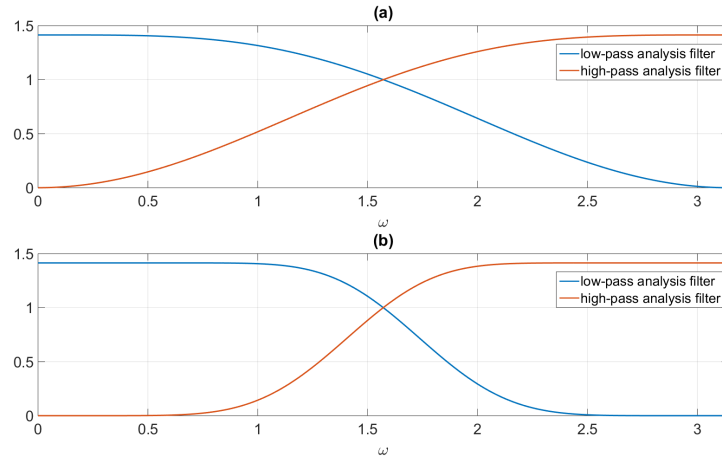


Fig. 6. Plot (a) shows the amplitude of the frequency response of the db2 DWT filters. Plot (b) shows the amplitude of the frequency response of the db8 DWT filters.

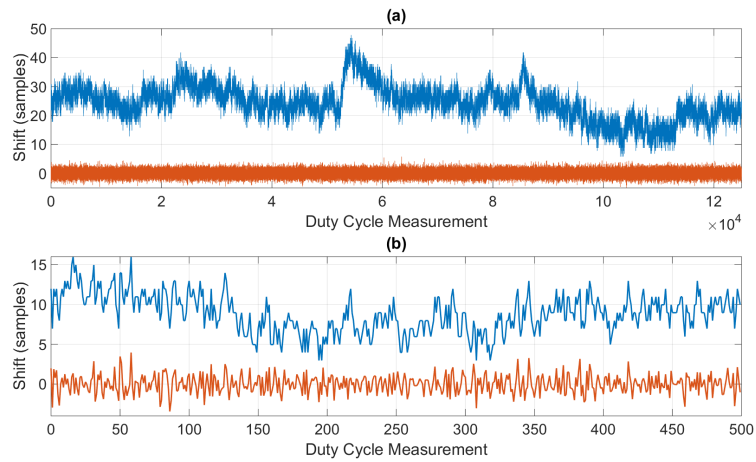


Fig. 7. Plot (a) shows long-term detrending. Plot (b) shows short-term detrending.

accurately approximate the true delay compared to the template. Finally, perform the same division and group delay calculations on the off event waveform means and detrend. Since deconvolution lifts the concern of voltage spike oscillations interfering with itself shifted in time, we removed the low-pass filter added earlier for a more general solution that applies to any type of signal.

By combining the deconvolution and detrending techniques, we were able to extract the last round key of an implementation of AES with 1.30×10^5 unique inputs over 2 days and 20 hours, with 1,000 averaged traces for each unique trace. Using the same data with only deconvolution or detrending yielded one correct sub-key byte from the last round key. No deconvolution or detrending yielded no correct sub-key bytes.

We present a summary of the results of our attacks in Table 2. The straightforward approach is one where no signal processing is applied and one can extract bytes of the key. However, as shown, using detrending and deconvolution allow for a much more efficient attack.

Table 2. A summary of the results presented in Section 5, comparing a straightforward (no signal processing) with the use of detrending and deconvolution. The Bytes column represents the number of bytes of AES key that could be extracted from the acquired traces.

Method	Acquisitions	Averaging	Time / hours	Bytes
Straightforward	1.85×10^5	2^{16}	142	1
Detrending	1.25×10^5	2^{16}	96	1
Deconvolution	1.30×10^5	2^{10}	68	1
Detrending & Deconvolution	1.30×10^5	2^{10}	68	16

6 Conclusions

In this paper we demonstrated that an attacker can derive information from the duty cycle of the primary side of an SMPS. We first demonstrated how leakage detection methods can be used and how improving the SNR increases the t -statistic. This led to a straightforward attack on the primary side of an SMPS using CPA, but requires a significant number of traces per byte of the subkey attacked. We then described techniques that could be used to increase the SNR. Specifically detrending and deconvolving the acquisitions that allowed for the extraction of a full AES subkey using fewer traces than that required for a single subkey byte in the straightforward case. Our experimental results demonstrate that our attack can be applied at some distance from the device, i.e. an attacker does not need direct access to a device, but could monitor it from a wall-mounted transformer.

We note the techniques described were used to derive information from an integrated measurement and could be applied to other side channel attacks using

other types of signals. For example, by detrending sample points within a trace over multiple traces, one could remove the influence of hardware blocks operating asynchronously to the signal of interest. For signals that are difficult to align because of amplitude noise, yet changing in frequency due from timing jitter, one could collapse the trace, or portions of the trace, encapsulating a portion of a cryptographic operation in a single point. For algorithms with masking, one can derive methods for collapsing each trace, or portions of each trace, sacrificing SNR for a reduced search space. In many instances, the approach entails the sacrificing of SNR for some other gain, then performing techniques outlined in this paper in an attempt to recoup the SNR while maintaining the sought after advantage.

The approach taken in this paper focuses on reducing the time to extract an AES key rather than reducing the number of AES encryptions required to conduct an attack. An approach that focuses on the latter could involve performing a single AES encryption operation for each input data, and allowing multiple different encryptions to be performed within each SMPS duty cycle. One could then use the same set of acquisitions measuring the duty cycles to analyze multiple AES encryption operations, but with different weights that would shift and slide in time at the same rate. Using other techniques, such as principal component analysis (PCA), one could then find optimal weighting functions to maximize the information of each duty cycle for multiple inputs.

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A Voltage Spike Interpretation

By deducing the direction of current flow immediately following an SMPS switching event, one can determine, or predict, more information about the resulting voltage spike. Consider when an SMPS switches the primary from disconnected to connected, or *on*, as in Fig. 8. While disconnected, the secondary side will drop its potential as energy flows out of the low-pass filter into the load on the secondary side. On the primary side, current from the source powering the SMPS flows through the ESL into the capacitor. When the connection to the primary side reestablishes itself, the lower potential secondary side causes a sudden draw of current from the primary side that in turn suddenly reverses the flow of current through the ESL. The sudden change in current through the ESL induces a voltage opposite, or against, the voltage applied on the primary side. As such, an observer monitoring voltage upstream of the SMPS on the primary side will measure a sudden drop in voltage followed by a recovery based on the capacity of the capacitor and the capabilities of the source powering the SMPS.

Similarly, consider when an SMPS switches the primary from connected to disconnected, or *off*, as in Fig. 9. While connected, the secondary side draws current from the capacitor and the source powering the SMPS. When the SMPS disconnects from the primary, the current flowing out of the capacitor and through

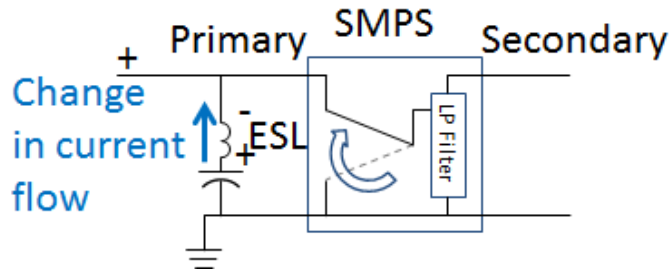


Fig. 8. SMPS with primary connecting.

the ESL suddenly changes direction when all the current from the source feeds, or replenishes, the capacitor. The sudden change in current in turn generates a voltage aligned, or in addition to, the voltage applied on the primary side. As such, an observer monitoring voltage upstream of the SMPS on the primary side will see a sudden increase in voltage followed by a recovery based on the capacity of the capacitor and the source powering the SMPS.

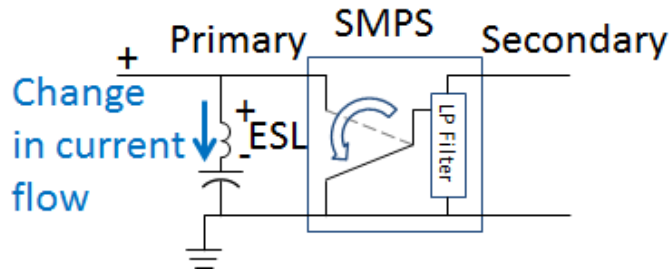


Fig. 9. SMPS with primary disconnecting.

Discriminating between on and off switching events from the primary side of the SMPS reduces to a simple check of voltage polarity swing at the beginning of the voltage spike. Furthermore, the absolute amplitude of the voltage spike and recovery typically differ between on and off switching events for multiple reasons, including input voltage level, load and capacitance. The resulting signal allows for very straightforward triggering logic to capture voltage traces synchronous to an on or off switching event.

Our measurements taken do not employ any strategic tap location or additional conditioning on the power going to the primary side of the SMPS. While some data conditioning can clean the voltage signal to simplify measurements, such modifications entail more intrusive modifications than a simple direct tap at the source for the SMPS. Only minimal signal conditioning was used on the

tapped line fed to a signal recorder. In fact, to emphasize the ability to monitor power usage from a distance, all measurements taken come from a tap six feet away from the SMPS and co-located at the output of the power source feeding its primary side.

B Building Targeted Plaintext Vector and Secret Key

In this section we give a more explicit description of the method we detail in Section 3 to derive a plaintext vector and secret key. In the attack described in this paper the leakage from a device during the computation of one, or more, instances of a block cipher is summed to a single value. The Test Vector Leakage Assessment (TVLA), proposed by Goodwill et al. [9], uses a t -test to determine if a fixed input is distinguishable from a random input, as described in Section 3.

For a block cipher, one would want to construct test vectors where, at a chosen point in the computation, there is a minimal Hamming weight and a minimal Hamming distance from some previous state. These correspond to the leakage models typically observed in microprocessors [3], and will maximize the observed leakage. The chosen vectors, and the resulting ciphertexts, should also be indistinguishable from random values to avoid erroneous leakage detection.

We consider 128-bit AES as shown in Fig. 10 where a 128-bit plaintext $P = (p_0, p_1, \dots, p_{15})$ is used to compute a ciphertext $C = (c_0, c_1, \dots, c_{15})$. These are typically expressed as matrices:

$$P = \begin{pmatrix} p_0 & p_4 & p_8 & p_{12} \\ p_1 & p_5 & p_9 & p_{13} \\ p_2 & p_6 & p_{10} & p_{14} \\ p_3 & p_7 & p_{11} & p_{15} \end{pmatrix} \quad \text{and} \quad C = \begin{pmatrix} c_0 & c_4 & c_8 & c_{12} \\ c_1 & c_5 & c_9 & c_{13} \\ c_2 & c_6 & c_{10} & c_{14} \\ c_3 & c_7 & c_{11} & c_{15} \end{pmatrix}.$$

The plaintext is initially XORed with a first round key k_0 , equivalent to the secret key, and then a round function R is applied iteratively with a sequence of round keys. Each function R takes a state matrix, conducts a series of round operations (ShiftRows, ByteSub and MixColumns operations) and XORs the result with a round key (AddRoundKey operation).

In order to generate plaintext vectors and a secret key that can be used to detect leakage in the middle of a block cipher, one would proceed as follows:

1. Select one of the middle rounds, denoted i .
2. Choose a state s_1 , see Fig. 10, where $x_0 = 0$.
3. Determine a k_i , such that the output of the next round s_2 is also equal to s_1 .
4. Compute k_0 , the secret key, from k_i , given that the key schedule of AES is invertible.
5. Given k_0 and s_1 , decipher s_1 the required number of rounds to determine the plaintext P .
6. Note the plaintext P as the first test vector.

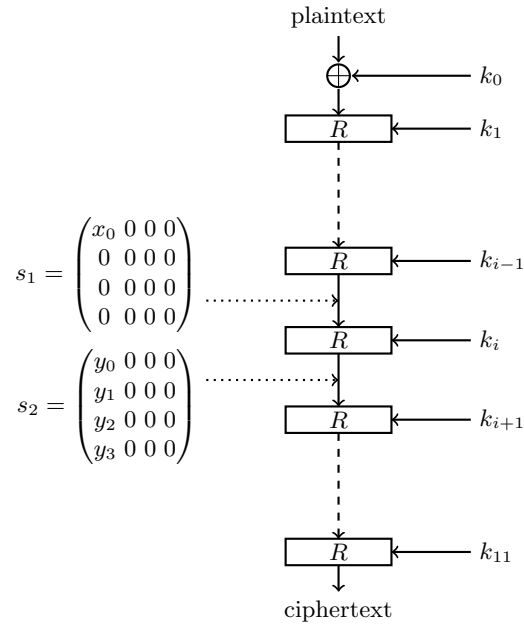


Fig. 10. The structure of AES, and the states chosen to determine plaintext vectors and a secret key for leakage detection.

7. Generate remaining entries in the test vector set as follows:
 - Choose a state s_1 , where $x_0 \in \{1, \dots, 255\}$.
 - Given k_0 and s_1 , decipher s_1 the required number of rounds to determine the plaintext P .
 - Note the plaintext P as another test vector.

The above would allow for 256 distinct plaintext elements to be generated. In the work described in this paper, two bytes of s_1 are varied to allow 2^{16} distinct plaintext elements to be generated.